DIGITAL SYSTEM DESIGN (EC303PC)

MOOCS SWAYAM NPTEL COURSE AS DIGITAL CIRCUITS

COURSE PLANNER

I. COURSE OVERVIEW:

The course will make them learn the basic theory of switching circuits and their applications in detail. Starting from a problem statement they will learn to design circuits of logic gates that have a specified relationship between signals at the input and output terminals. They will be able to design combinational and sequential circuits .They will learn to design counters, adders, sequence detectors. This course provides a platform for advanced courses like Computer architecture, Microprocessors & Microcontrollers and VLSI design. Greater Emphasis is placed on the use of programmable logic devices and State machines.

II. PREREQUISITS:

1. The Pre-requisites for this Course is basic Boolean algebra for Digital Electronic Circuits.

III. COURSE OBJECTIVES:

1.	To understand common forms of number representation in logic circuits
2.	To learn basic techniques for the design of digital circuits and fundamental concepts used in the design of digital systems.
3.	To understand the concepts of combinational logic circuits and sequential circuits.
4.	To understand the Realization of Logic Gates Using Diodes & Transistors.

IV. COURSE OUTCOMES:

S.No.	Description	Bloom's Taxonomy Level
1.	**Understand** the numerical information in different forms and Boolean Algebra theorems.	Understand(Level2)
2.	**Understand** Postulates of Boolean algebra and to minimize combinational functions.	Understand(Level2)
3.	**Design** and A**nalyze** combinational and sequential circuits.	Understand(Level2)

4.	**Know** about the logic families and realization of logic gates.	Knowledge, Understand (Level1, Level2)

V. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (PO)		Level	Proficiency assessed by
PO1	Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems related to Electronics & Communication and Engineering.	2	Lectures, Assignments, Exercises
PO2	Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems related to Electronics & Communication Engineering and reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Hands on Practice Sessions
PO3	Design/development of solutions: Design solutions for complex engineering problems related to Electronics & Communication Engineering and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Design Exercises, Projects
PO4	Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	1	Lab sessions, Exams
PO5	Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	1	Design Exercises, Oral discussions
PO6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the Electronics & Communication Engineering professional engineering practice.	-	-

Program Outcomes (PO)		Level	Proficiency assessed by
PO7	Environment and sustainability: Understand the impact of the Electronics & Communication Engineering professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	-	-
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	-	-
PO9	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	3	Seminars Discussions
PO10	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	-	-
PO11	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	-	-
PO12	Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	2	Development of Mini Projects

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VI. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO 1	Professional Skills: An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	3	Lectures and Assignments
PSO 2	Problem-Solving Skills: An ability to solve complex Electronics and communication Engineering problems, using latest	2	Tutorials

	hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.		
PSO 3	Successful Career and Entrepreneurship: An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	3	Seminars and Projects

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VII. SYLLABUS:

Course syllabus: (JNTU)

UNIT - I: Number Systems: Number systems, Complements of Numbers, Codes- Weighted and Non-weighted codes and its Properties, Parity check code and Hamming code.

Boolean Algebra: Basic Theorems and Properties, Switching Functions- Canonical and Standard Form, Algebraic Simplification, Digital Logic Gates, EX-OR gates, Universal Gates, Multilevel NAND/NOR realizations.

UNIT - II: Minimization of Boolean functions: Karnaugh Map Method - Up to five Variables, Don't Care Map Entries, Tabular Method, **Combinational Logic Circuits:** Adders, Subtractors, Comparators, Multiplexers, Demultiplexers, Encoders, Decoders and Code converters, Hazards and Hazard Free Relations.

UNIT - III: Sequential Circuits Fundamentals: Basic Architectural Distinctions between Combinational and Sequential circuits, SR Latch, Flip Flops: SR, JK, JK Master Slave, D and T Type Flip Flops, Excitation Table of all Flip Flops, Timing and Triggering Consideration, Conversion from one type of Flip-Flop to another.

Registers and Counters: Shift Registers – Left, Right and Bidirectional Shift Registers, Applications of Shift Registers - Design and Operation of Ring and Twisted Ring Counter, Operation of Asynchronous and Synchronous Counters.

UNIT - IV : Sequential Machines: Finite State Machines, Synthesis of Synchronous Sequential Circuits- Serial Binary Adder, Sequence Detector, Parity-bit Generator, Synchronous Modulo N –Counters. Finite state machine-capabilities and limitations, Mealy and Moore models.

UNIT - V: Realization of Logic Gates Using Diodes & Transistors: AND, OR and NOT Gates using Diodes and Transistors, DCTL, RTL, DTL, TTL, CML and CMOS Logic Families and its Comparison, Classification of Integrated circuits, comparison of various logic families, standard TTL NAND Gate Analysis & characteristics, TTL open collector O/Ps, Tristate TTL, MOS & CMOS open drain and tristate outputs, CMOS transmission gate, IC interfacing- TTL driving CMOS & CMOS driving TTL.

TEXT BOOKS:

1. Switching and Finite Automata Theory- Zvi Kohavi & Niraj K. Jha, 3rdEdition,Cambridge . 2. Modern Digital Electronics – R. P. Jain, 3rd Edition, 2007- Tata McGraw-Hill

REFERENCE BOOKS:

1. Digital Design- Morris Mano, PHI, 4th Edition,2006
2. Introduction to Switching Theory and Logic Design – Fredriac J. Hill, Gerald R. Peterson, 3rd Ed, John Wiley & Sons Inc.
3. Fundamentals of Logic Design- Charles H. Roth, Cengage Learning, 5th, Edition, 2004.
4. Switching Theory and Logic Design – A Anand Kumar, PHI, 2013

NPTEL Web Course: Digital Circuits

NPTEL Video Course: Digital Circuits

GATE Syllabus: Digital Circuits, Number systems; Combinatorial circuits: Boolean algebra, minimization of functions using Boolean identities and Karnaugh map, logic gates and their static CMOS implementations, arithmetic circuits,code converters, multiplexers, decoders and PLAs; Sequential circuits: latches and flip-flops, counters, shift-registers and finite state machines;

IES Syllabus:Digital Circuits (Section:6)Boolean Algebra& uses; Logic gates, Digital IC families, Combinatorial/sequential circuits; Basics of multiplexers, counters/registers/ memories /microprocessors, design& applications.

VIII. COURSE PLAN (WEEK-WISE):

Lecture No.	Week	Topics to be covered	Link for PPT	Link for PDF	Link for Small Projects/ Numericals(if any)	Course learning outcomes	Teaching Methodology	Reference
1	Week-1	Introduction	https://drive.google.com/file/d/1EI6ICoaZJxT0mX5J6Rcrsji5HEG8xe-j/view?usp=sharing	https://drive.google.com/file/d/1MrXyqjUBvlcELBXSXV46_E3pP9iKUhvt/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know the digital signal and digital system	1. Chalk&Board 2. ICT	1. R. P. Jain, "Modern Digital Electronics", McGraw Hill Education, 2009 2. M. M. Mano, "Digital logic and Computer design", Pearson Education India, 2016
2		Number systems, Number systems convesion	https://drive.google.com/file/d/1EI6ICoaZJxT0mX5J6Rcrsji5HEG8xe-j/view?usp=sharing	https://drive.google.com/file/d/1MrXyqjUBvlcELBXSXV46_E3pP9iKUhvt/view?usp=sharing	Small Projects/ Numericals(if any) Link	To Know and understand the different number systems and number systems conversion	1. Chalk&Board 2. ICT	

3		Complements of Numbers	https://drive.google.com/file/d/1zDLWsZI25RfSfmN7FGrbKswBq-bxIH0L/view?usp=sharing	https://drive.google.com/file/d/18cclOkCWgz7G617y3LCk7slLmSgvxSGI/view?usp=sharing	Small Projects/ Numericals(if any) Link	To Know and understand the complements	1. Chalk&Board 2. ICT	
4		Codes- Weighted and Non-weighted codes, Binary codes: Properties	https://drive.google.com/file/d/1aKg89h4-tPJO9T60ItwPRuXhLRVOhRWQ/view?usp=sharing	https://drive.google.com/file/d/1CKxIcjrtzWkU05yOdpmqB8wsrSmeEVrI/view?usp=sharing	Small Projects/ Numericals(if any) Link	To Know Binary codes and To understand the gray code	1. Chalk&Board 2. ICT	
5	Week-2	Parity check code and Hamming code	https://drive.google.com/file/d/1aKg89h4-tPJO9T60ItwPRuXhLRVOhRWQ/view?usp=sharing	https://drive.google.com/file/d/1CKxIcjrtzWkU05yOdpmqB8wsrSmeEVrI/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand the error correction and detection	1. Chalk&Board 2. ICT	
6		Boolean Algebra: Basic Theorems and Properties	https://drive.google.com/file/d/1lSLGQ3om82issBoNIkEHJv5Bjp5CfL95/view?usp=sharing	https://drive.google.com/file/d/1zF13wPQjTTWc7CpfMEcH5Y14_in947_U/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand the Boolean logic	1. Chalk&Board 2. ICT	
7		Switching Functions- Canonical and Standard Form, Algebraic Simplification	https://drive.google.com/file/d/1ATZauI994Ik6OEBydvUU_I2m0Uw1Xt0Q/view?usp=sharing	https://drive.google.com/file/d/1OIQQbyVW61adSJIoyAPyNUuFAY0raAEU/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand the switching function	1. Chalk&Board 2. ICT	
8		Digital Logic Gates, EX-OR gates, Universal Gates, NAND/NOR realizations	https://drive.google.com/file/d/1ko35m3-f5dBgMYkyuSSbKYnz5y_YJKjH/view?usp=sharing	https://drive.google.com/file/d/1u74CJgVltHHKZcu6RgXP6Gl2F86bP9cX/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know the XOR properties, To know and understand the universal gates	1. Chalk&Board 2. ICT	
9	Week-3	Minimization of Boolean functions: Introduction, Karnaugh Map Method - Up to five Variables, Don't Care Map Entries	https://drive.google.com/file/d/1lSLGQ3om82issBoNIkEHJv5Bjp5CfL95/view?usp=sharing	https://drive.google.com/file/d/1zF13wPQjTTWc7CpfMEcH5Y14_in947_U/view?usp=sharing	Small Projects/ Numericals(if any) Link	To Know and understand the Boolean postulates, To Analyze the Karnaugh Map	1. Chalk&Board 2. ICT	

10		Tabular Method	https://drive.google.com/file/d/1lSLGQ3om82issBoNIkEHJv5Bjp5CfL95/view?usp=sharing	https://drive.google.com/file/d/1zF13wPQjTTWc7CpfMEcH5Y14_in947_U/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand the Quine-McKluskey Algorithm	1. Chalk&Board 2. ICT	
11		Student Presentation				To know student communication skills	1. Chalk&Board 2. ICT	
12		Mocktest-1				To know student understanding in unit-1	1. Chalk&Board 2. ICT	
13	Week-4	Combinational Logic Circuits: Introduction	https://drive.google.com/file/d/1_RS17x6yyIln1kylzyAEux7c7pXzCOKN/view?usp=sharing	https://drive.google.com/file/d/1ts2LiD6I6iWazlXicEzk_efddLwgTpM5/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know Combinational circuits	1. Chalk&Board 2. ICT	
14		Adders	https://drive.google.com/file/d/1_RS17x6yyIln1kylzyAEux7c7pXzCOKN/view?usp=sharing	https://drive.google.com/file/d/1ts2LiD6I6iWazlXicEzk_efddLwgTpM5/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design Binary adder	1. Chalk&Board 2. ICT	
15		Subtractors	https://drive.google.com/file/d/1_RS17x6yyIln1kylzyAEux7c7pXzCOKN/view?usp=sharing	https://drive.google.com/file/d/1ts2LiD6I6iWazlXicEzk_efddLwgTpM5/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design Binary subtractor	1. Chalk&Board 2. ICT	
16		Bridge class-1/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT	
17	Week-5	Comparators				To design Binary comparator	1. Chalk&Board 2. ICT	1. R. P. Jain, "Modern Digital Electronics", McGraw Hill Education, 2009 2. M. M. Mano, "Digital logic and Computer design", Pearson Education India, 2016
18		Multiplexers, Demultiplexers	https://drive.google.com/file/d/14sMUV4Dpdop1ByDgLnb_JlXhbf8NeVbq/view?usp=sharing	https://drive.google.com/file/d/1Yn0uO13uVJZkViq1KcI3E_sK241j53OE/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand multiplexer & Demultiplexer	1. Chalk&Board 2. ICT	
19		Encoders, Decoders				To design Encoder, Decoders	1. Chalk&Board 2. ICT	
20		Bridge class-2/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT	

21		Code converters	https://drive.google.com/file/d/1EA4lLWupuwbeSR_A--EsmrcCyc6yU2UD/view?usp=sharing	https://drive.google.com/file/d/1HL62DbewWNLKTuZzhdEd-6t-EL33e-HR/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design code converters	1. Chalk&Board 2. ICT
22	Week-6	Hazards, Hazard Free Relations	https://drive.google.com/file/d/1EA4lLWupuwbeSR_A--EsmrcCyc6yU2UD/view?usp=sharing	https://drive.google.com/file/d/1HL62DbewWNLKTuZzhdEd-6t-EL33e-HR/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand static hazards	1. Chalk&Board 2. ICT
23		Student Presentation				To know student communication skills	1. Chalk&Board 2. ICT
24		Bridge class-3/Student Presentation				To cover subject knowledge gap	1. Chalk&Board2. ICT
25	Week-7	Sequential Circuits Fundamentals: Basic Architectural Distinctions between Combinational and Sequential circuits	https://drive.google.com/file/d/1e0QdFCNzxqP62LM7J6h6ESaC1dJRmnz_/view?usp=sharing	https://drive.google.com/file/d/1l_2zVHzBxkhRwf2OVVl8w0c-71EN12pc/view?usp=sharing	Small Projects/ Numericals(if any) Link	To Know and understand the sequential circuits	1. Chalk&Board 2. ICT
26		SR Latch, Flip Flops: SR, JK	https://drive.google.com/file/d/1e0QdFCNzxqP62LM7J6h6ESaC1dJRmnz_/view?usp=sharing	https://drive.google.com/file/d/1l_2zVHzBxkhRwf2OVVl8w0c-71EN12pc/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand the operation of latch	1. Chalk&Board 2. ICT
27		JK Master Slave, D and T Type Flip Flops	https://drive.google.com/file/d/1liDhsuNdJ3tIo1keu4HqfLI_J_bGZcwb/view?usp=sharing	https://drive.google.com/file/d/1TMa2r7V4EQyGzYT7zTyIw5NqTE0oFon-/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand different flip flops	1. Chalk&Board 2. ICT
28		Bridge class-4/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT

29		F/F Characteristic, Excitation Table	https://drive.google.com/file/d/1RJ5Fgx6NQTFXcyVyMkdsutOjNpniyFiw/view?usp=sharing	https://drive.google.com/file/d/1KBIlG0E5DZZe0yaXrKZ1xoJR64iFUT5L/view?usp=sharing	Small Projects/ Numericals(if any) Link	To analyze characteristic, excitation table	1. Chalk&Board 2. ICT
30	Week-8	Timing and Triggering Consideration	https://drive.google.com/file/d/1ftid4Gux3rQPp_MVmXgoPoeOsUnR-_2u/view?usp=sharing	https://drive.google.com/file/d/1ZkFiWExOeoxlUKhhnhRcCzA0ko1O1xUy/view?usp=sharing	Small Projects/ Numericals(if any) Link	To analyze the timing issues	1. Chalk&Board 2. ICT
31		Conversion from one type of Flip-Flop to another	https://drive.google.com/file/d/13sLpyBt2EZu0EIQZxDA3oe6ySUQKtQOc/view?usp=sharing	https://drive.google.com/file/d/1-eMOLPGWHfS0nITGK9FdzUgsyatYQPgv/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand flip-flop conversion	1. Chalk&Board 2. ICT
32		Bridge class-5/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT
33	Week-9	Registers and Counters: Shift Registers	https://drive.google.com/file/d/1ftid4Gux3rQPp_MVmXgoPoeOsUnR-_2u/view?usp=sharing	https://drive.google.com/file/d/1ZkFiWExOeoxlUKhhnhRcCzA0ko1O1xUy/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand shift register	1. Chalk&Board 2. ICT
34		Left, Right and Bidirectional Shift Registers	https://drive.google.com/file/d/13sLpyBt2EZu0EIQZxDA3oe6ySUQKtQOc/view?usp=sharing	https://drive.google.com/file/d/1-eMOLPGWHfS0nITGK9FdzUgsyatYQPgv/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design Left, Right and Bidirectional Shift Registers	1. Chalk&Board 2. ICT
35		Applications of Shift Registers	https://drive.google.com/file/d/14XE3OQY2BQN0GyeGGdPrG6h_hfJCATnC/view?usp=sharing	https://drive.google.com/file/d/12aBGuzj3jWfA3MvsGAqNjNPZnD2y8K2T/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design shift Registers	1. Chalk&Board 2. ICT
36		Bridge class-6/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT

37		Design and Operation of Ring and Twisted Ring Counter	https://drive.google.com/file/d/1z_mVDaBtPm0EJ3bgDlEyhmBCyqtzl2ZU/view?usp=sharing	https://drive.google.com/file/d/1H-8DehaFb96_OsAWalTvVkHViZ5vI4RA/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know shift register applications	1. Chalk&Board 2. ICT
38	Week-10	Operation of Asynchronous & Synchronous Counters	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know Asynchronous Counters	1. Chalk&Board 2. ICT
39		Student Presentation				To know student communication skills	1. Chalk&Board 2. ICT
40		Bridge class-7/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT
41	Week-11	Sequential Machines: Finite State Machines	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know Finite State Machines	1. Chalk&Board 2. ICT
42		Synthesis of Synchronous Sequential Circuits, Serial Binary Adder	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To analyze Synchronous Sequential Circuits, To understand Serial Binary Adder	1. Chalk&Board 2. ICT
43		Sequence Detector	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand Sequence Detector	1. Chalk&Board 2. ICT
44		Bridge class-8/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT

45		Parity-bit Generator, Synchronous Modulo N –Counters	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand Parity-bit Generator, To design Modulus Counters	1. Chalk&Board 2. ICT
46	Week-12	Finite state machine-capabilities and limitations	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand FSM capabilities	1. Chalk&Board 2. ICT
47		Mealy and Moore models	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know FSM models	1. Chalk&Board 2. ICT
48		Bridge class-9/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT
49	Week-13	Mock Test-2				To know student understanding in unit-4	1. Chalk&Board 2. ICT
50		Realization of Logic Gates Using Diodes & Transistors: Introduction	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design logic gates using discrete components	1. Chalk&Board 2. ICT
51		AND, OR and NOT Gates using Diodes and Transistors	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design logic gates using discrete components	1. Chalk&Board 2. ICT
52		Bridge class-10/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT

53		DCTL, RTL, DTL,TTL, CML	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To design logic gates using discrete components	1. Chalk&Board 2. ICT
54	Week-14	CMOS Logic Families	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know the CMOS logic	1. Chalk&Board 2. ICT
55		Logic Families Comparison, Classification of Integrated circuits	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know the logic families merits and demerits, To know integrated circuits	1. Chalk&Board 2. ICT
56		Bridge class-11/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT
57	Week-15	standard TTL NAND Gate-Analysis & characteristics	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand TTL NAND	1. Chalk&Board 2. ICT
58		TTL open collector O/Ps, Tristate TTL	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand open collector	1. Chalk&Board 2. ICT
59		MOS & CMOS open drain and tristate outputs	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand MOS open drain	1. Chalk&Board 2. ICT
60		Bridge class-12/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT

61		CMOS transmission gate	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To understand transmission gate	1. Chalk&Board 2. ICT
62	Week-16	IC interfacing- TTL driving CMOS, CMOS driving TTL	https://drive.google.com/file/d/1l6iP4Djjwi7pHdDzI2TYAu0EtHYJF9Xm/view?usp=sharing	https://drive.google.com/file/d/17BPlOmFRslwmLEeYUoHg5CL3sr9a9eat/view?usp=sharing	Small Projects/ Numericals(if any) Link	To know IC interfacing	1. Chalk&Board 2. ICT
63		Student Presentation				To know student communication skills	1. Chalk&Board 2. ICT
64		Bridge class-13/Student Presentation				To cover subject knowledge gap	1. Chalk&Board 2. ICT

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	PO 1	PO2	PO3	PO 4	PO 5	PO6	PO 7	PO8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CO1	3	3	1	2	1	-	-	-	3	-	-	2	3	2	3
CO2	3	3	3	1	2	-	-	-	3	-	-	1	3	1	3
CO3	1	2	3	1	1	-	-	-	3	-	-	2	3	2	3
CO4	1	1	3	1	1	-	-	-	3	-	-	1	3	1	3
Average	2	2.25	2.5	1.25	1.25	-	-	-	3	-	-	1.5	3	1.5	3
Rounded Average	2	2	3	1	1	-	-	-	3	-	-	2	3	2	3

1: Slight (Low) **2**: Moderate (Medium) **3**: Substantial (High) - : None

X. QUESTION BANK (JNTUH) :

UNIT - I

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Write the steps involved in unsigned binary subtraction using complements with examples.	Remember	1
2.	a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend: i. 100-110000 ii. 11010-1101 (b) Construct a table for 4321 weighted code and write 9154 using this code.	Apply	1
3.	Find $(3250\text{-}72532)_{10}$ using 10's complement.	Apply	1
4.	(a) Perform arithmetic operation indicated below. Follow signed bit notation i. 001110 + 110010 ii. 101011-100110	Apply	1
5.	(a)Divide 01100100 by 00011001 (b)Given that $(292)_{10}=(1204)_b$ determine 'b'	Apply	1
6.	(a) What is the gray code equivalent of the Hex Number 3A7(b)Find the binary number code for the decimal numbers from 0 to 9(c) Find 9's complement $(25.639)_{10}$	Understand	1
7.	(a)Find (72532-03250)using 9's complement. (b) Show the weights of three different 4 bit self complementing codes whose only negative weight is -4 and write down number system from 0 to 9.	Apply	1
8.	Decimal system became popular because we have 10 fingers. A rich person on Earth has decided to distribute Rs. One lakh equally to the following persons from various planets. Find out the amount each one of them will get in their respective currencies: A from planet VENUS possessing 8 fingers B from planet MARS possessing 6 fingers	Apply	1

	C from planet JUPITER possessing 14 fingers D from MOON possessing 14 fingers		
9.	State and prove any 4 Boolean theorems with examples	Understand	1
10.	(a) Simplify to a sum of 3 terms: A'C'D' + AC' +BCD + A'CD' + A'BC + AB'C' (b) Given AB' + AB =C, show that AC' + A'C =B	Apply	1

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Write short notes on binary number systems.	Remember	1
2.	Discuss 1"s and 2"s complement methods of subtraction.	Understand	1
3.	Discuss octal number system.	Understand	1
4.	State and prove transposition theorem.	Apply	1
5.	Show how do you convert AND logic to NAND logic?	Apply	1
6.	Describe a short note on five bit bcd codes.	Remember	1
7.	Illustrate about unit –distance code? State where they are used.	Understand	1
8.	State about error correcting codes?	Remember	1
9.	When do you say that a signal is asserted?	Understand	1
10.	State about logic design and what do you mean by positive logic system?	Understand	1

UNIT - II

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	A combinational circuit has 4 inputs (A,B,C,D) and three outputs (X,Y,Z). XYZ represents a binary number whose value equals the number of 1's at the input	Evaluate	2

	i. Find the minterm expansion for the X,Y, Z ii. Find the maxterm expansion for the Y and Z.		
2.	A combinational circuit has four inputs (A, B, C ,D), which represent a binary-coded-decimal digit. The circuit has two groups of four outputs- S,T, U, V (MSB digit) and W, X,Y,Z (LSB digit). Each group represents a BCD digit. The output digits represent a decimal number which is five times the input number. Write down the minimum expression for all the outputs.	Evaluate	2
3.	Simplify the following Boolean expressions using K-map and implement them using NOR gates: (a) F (A, B, C D) = AB'C'+ AC +A'CD' (b)F (W, X, Y,Z)= W' X' Y' Z'+ WXY'Z'+ W'X'YZ+WXYZ	Analyze	2
4.	Design BCD to Gray code converter and realize using logic gates.	Analyze	2
5.	Design 2*4 decoder using NAND gates.	Analyze	2
6.	Reduce the following expression using K-map (BA+A'B+AB')	Apply	2
7.	Design a circuit with three inputs (A, B, C) and two outputs (X,Y) where the outputs are the binary count of the number of "ON" (HIGH) inputs	Analyze	2
8.	A certain 4 input gate called LEMON gate relizes the switching function LEMON (A,B,C,D) = BC(A+D). Assuming that the input variables are available in both primed and unprimed form:	Analyze	2
9.	Show a realization of the function f(w,x,y,z)= ∑(0,1,6,9,10,11,14,15) with only 3 LEMON B gate and one OR gate.	Apply	2
10.	Design a circuit with four inputs and one output where the output is ! if the input is divisible by 3 or 7.	Analyze	2

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Define K-map?	Remember	2
2.	Write the block diagram of 2-4 and 3-8 decoders?	Understand	2
3.	Define magnitude comparator?	Remember	2
4.	What do you mean by look-ahead carry?	Remember	2
5.	Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z using K-map	Apply	2
6.	How combinatorial circuits differ from sequential circuits?	Understand	2
7.	What are the IC components used to design combinatorial circuits with MSI and LSI?	Understand	2
8.	Define the importance of prime implications	Understand	2
9.	Locate the minters in a three variable map for f=∑m(0,1,5,7)	Apply	2
10.	Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z without using K-map	Apply	2

UNIT - III

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Compare RS and JK flip flop.	Evaluate	3
2.	Describe about T flip flop with the help of a logic diagram and characteristic table. Derive a T-flip-flop from JK and D flip flop.	Understand	3
3.	Differentiate combinational and sequential circuits.	Understand	3
4.	Explain the working principle of JK flip flop in detail.	Understand	3
5.	Derive a JK-flip-flop from SR flip flop.	Create	3
6.	Explain serial transfer in 4-bit shift registers	Understand	3

7.	Explain about Binary Ripple counter.	Understand	3
8.	Define Latch. Explain different types of Latches in detail	Understand	3
9.	Examine with the help of a block diagram , the basic components of a sequential circuit.	Understand	3
10.	Explain the Ripple counter design. Mention its application	Understand	3

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Distinguish between a shift register and counter?	Understand	3
2.	What are the applications of shift registers?	Understand	3
3.	What are the applications of Flip-Flops?	Understand	3
4.	Discuss about a bidirectional shift register?	Understand	3
5.	How do you build a latch using universal gates?	Analyze	3
6.	What is the flip-flop memory characteristic?	Understand	3
7.	Distinguish between synchronous and asynchronous latch?	Understand	3
8.	What is meant by clocked flip-flop?	Understand	3
9.	Why a gated D latch is called a transparent latch?	Understand	3
10.	What are the two types of flip-flops?	Understand	3

UNIT - IV

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Explain the design of sequential circuit with an example. Show the state reduction, State assignment.	Understand	3
2.	Define BCD counter and Draw its state table.	Remember	3
3.	Design a sequential circuit with two D flip flops A and B. and	Create	3

	one input x, when x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transition from 00 to 11 to 11 to 10 back to 00 and repeats.		
4.	Design a Modulo 12 up Synchronous counter using T flip flops and draw the circuit diagram	Create	3
5.	Design a decade counter.	Create	3
6.	Design a left shift and riht shift for the following data 10110101	Create	3
7.	Design a serial binary adder using state diagram.	Create	3
8.	Design a parity bit generator using state diagram.	Create	3
9.	Design a sequence detector for sequence 1110.	Create	3
10.	Design a 4-bit asynchronous counter using FSM.	Create	3

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	What is state diagram? Give an example.	Understand	3
2.	Distinguish Synchronous and asynchronous counter.	Understand	3
3.	What are the approaches to the Design of Synchronous Sequential Finite State Machines	Understand	3
4.	Discuss about serial binary adder.	Understand	3
5.	Draw the state diagram of a sequence detector for sequence 1010.	Understand	3
6.	Discuss about parity bit generator.	Understand	3
7.	Design a mod-3 counter.	Create	3
8.	What are the advantages and disadvantages of acynchronous counters?	Understand	3
9.	What do you mean by terminal count?	Understand	3

10.	State variable modulus counter?	Understand	3

UNIT - V

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation	Understand	4
2.	Design a 4 input CMOS OR-AND INVERT gate. Explain the circuit with the help of logic dig and function table	Create	4
3.	Explain the CMOS circuit behavior with resistive load	Create	4
4.	Explain the CMOS circuit behavior with resistive load voltage TTL and low voltage	Create	4
5.	What is interfacing? Explain interfacing between low voltage TTL and low voltage	Create	4

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Differentiate between the TTL and DTL logic families.	Understand	4
2.	Write about the TTL to CMOS interfacing	Understand	4
3.	Discuss about the fastest logic family and mention the typical values of its various	Remember	4

OBJECTIVE QUESTIONS:

UNIT-1

1. The fraction $(0.68)_{10}$ is equal to [ ]

a) $(0.010101)_2$ b) $(0.101)_2$ c) $(0.10101)_2$ d) $(0.10111)_2$

2. The Hexadecimal number A0 has the decimal value [ ]

a)80 b) 256 c) 100 d) 160

3. Given two numbers A & B in sign magnitude representation in an eight bit format A=00011110 & B=10011100, A XOR B gives [ ]

a)10000010 b) 00011111 c) 10011101 d) 11100001

4. The value of binary 1111 is [ ]

a) 2^3-1 b) 2^4-1 c) 2^4 d) none of these

5. The minimum number of bits required to represent negative numbers in the range of -1 to -11 using 2's complement arithmetic is [ ]

(a) 2 (b) 3 (c) 4 (d) 5

6. The following code is not a BCD code. [ ]

a) Gray code (b) Xs-3 code (c) 8421 code (d) All of these

7. A 15-bit hamming code requires [ ]

(a) 4 parity bits (b) 5 parity bits (c) 15 parity bits (d) 7 parity bits

8. If=5, thebase (radix) of the number system is [ ]

a) 5 (b) 6 (c) 7 (d) 8

9. The hexadecimal number system is used in digital computers and digital systems to [ ]

(a) Perform arithmetic operations (b) Perform logic operations

(c) Perform arithmetic and logic operations (d) Input binary data into the sys

10. Determine the value of base x if: $(211)_x = (152)_8$ [ ]

(a) 2 (b) 10 (c) 8 (d) 7

11. Determine the value of base x, if $(193)_x = (623)_8$ [ ]

(a) 16 (b) 4 (c) 2 (d) 5

12. Which of the following are called Universal gates [ ]

(a) NAND, NOR (b) AND, OR (c) XOR XNOR (d) OR, XOR

13. Indicate which of the following logic gates can be used to realized all possible combinational logic functions. **GATE1989 [ ]**

(A) OR gate **(B)**NAND gates only **(C)** EX-OR gate **(D)** NOR & NAND gates

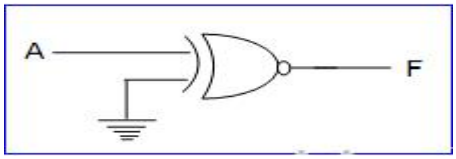
14. Boolean expression for the output of XNOR logic gate with inputs A and B is **GATE 1993 [ ]**

(A) AB' + A'B **(B)**(A(B)' + AB**(C)** (A' + (B)(A + B') **(D)** (A' + B')(A + B)

15. The output of a logic gate is '1' when all its inputs are at logic '0'. The gate is either **GATE 1994 [ ]**

(A)a NAND or an EX-OR gate **(B)**a NOT or an EX-NOR gate
(C)an OR or an EX-NOR gate (D)an AND or an EX-OR gate

16.The output of the logic gate shown is **GATE 1997 [ ]**



(A) 0 **(B)** 1 **(C)** A **(D)** A'

17. 2's complement representation of a 16 bit number (one sign bit and 15 magnitude bits) is FFFF. Its magnitude in decimal representation is **GATE 1993[ ]**

(A)0 **(B)** 1 **(C)** 32,767 (D) 65,535

18.Two 2's complement numbers having sign bits x and y are added and the sign bit of the result is z. Then, the occurrence of overflow is indicated by the Boolean function.

GATE 1998 [ ]

A) xyz (B) $\overline{x}\,\overline{y}\,\overline{z}$ (C) $\overline{x}\,\overline{y}z + xy\,\overline{z}$ (D)xy + yz + zx

19.4 – bit 2's complement representation of a decimal number is 1000. The number is

GATE 2002[ ]

(A) +8 **(B)** 0 **(C)** -7 **(D)** -8

20.The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) form is _____. **GATE 2014[ ]**

(A) 4 **(B)** 3 **(C)**2 **(D)** 8

21. Cyclic codes are also called _____codes

22. The basic two types of BCD codes are _____and_____ codes.

23. The distance between code words 10010 & 10101 is _____.

24. Convert the binary code (110110)2 to Gray code _____

25. Conversion of 0.1289062 decimal number to its hexa equivalent is _____

26. In b's complement method, the carry is _____ and in(b-1)'s complement method the carry is _____

27. The MSB of a binary number has a weight of 512, the number consists of _____ bits.

28. _____ are codes which represent letters of the alphabets and decimal numbers as a sequence of 0s and 1s.

UNIT-2

1.The short hand notation of min term m_6 is [ ]

(a) (b) (c) ABC (d)

2. In Boolean algebra A+AB= _____

3. Boolean expression xy+yz+ = _____on reduction.

4. The given expression Y=A+AB+ABC in SOP form is _____

5. In K-map each of the cell represents one of the _____ possible products [ ]

(a)2^n (b)2^{-n} (c)n^2 (d)All the above

6. The minimum number of bits required to represent negative numbers in the range of -1 to -11 using 2's complement arithmetic is [ ]

(a)2 (b) 3 (c) 4 (d) 5

7. The following code is not a BCD code. [ ]

a)Gray code (b) Xs-3 code (c) 8421 code (d) All of these

8. A 15-bit hamming code requires [ ]

(a)4 parity bits (b) 5 parity bits (c) 15 parity bits (d) 7 parity bits

9. The logic expression (A+B)(+) can be implemented by giving the inputs A and B to a two-input [ ]

(a)NOR gate (b) NAND gate (c) X-OR gate (d) X-NOR gate

10. Which of the following Boolean algebraic expressions is incorrect? [ ]

(a)A+B=A+B (b) A+AB=B (c) (A+B)(A+C)=A+BC (d) (A+)(A+B)=A

11. The hexadecimal number system is used in digital computers and digital systems to []

(a) Perform arithmetic operations (b) Perform logic operations

(c) Perform arithmetic and logic operations (d) Input binary data into the system.

12. The logic expression A+B can be implemented by giving inputs A and B to a two-input [ ]

(a)NOR gate (b) NAND gate (c) X-OR gate (d) X-NOR gate

13. A gate is enabled when its enable input is at logic 0. The gate is []

(a)NOR (b) AND (c) NAND (d) None of these

14. The output of a logic gate is 1 , when all its inputs are at logic 0.The gate is either [ ]

(a)a NOR or an X-NOR (b) a NAND or an X-OR

(c) an OR or an X-NOR (d) an AND or an X-OR

15. In b's complement method, the carry is _____and in(b-1)'s complement method the carry _____

16. The MSB of a binary number has a weight of 512,The number consists of _____

17._____ are codes which represent letters of the alphabets and decimal numbers as a sequence of 0s and 1s.

18. The interconnection of gates to perform a variety of logical operations is called_____

19. The NOR gate can function as a NOT gate if _____

20. The implicants which will definitely occur in the final expression are called_____

21. The prime implicant mode of a bunch of 0s is called a _____

22._____ is a process of converting familiar numbers or symbols into a coded format.

23. A decoder with 64 output lines has _____ select lines.

24. A decimal – to – BCD encoder is a ____ line to _____line encoder.

UNIT-3

1. The combinational circuits are_____ than sequential circuits [ ]
   A)slower **B)** faster **C)** same speed **D)** None

2. In combinational circuits the o/p depends on _____i/p [ ]
   A)present **B)** past **C)** A & B **D)** None

3. Full adder circuit adds _____number of bits at a time [ ]
A) 5 **B)** 2 **C)** 5 **D)** 3

4. Half adder circuit adds _____number of bits at a time [ ]
A) 5 **B)** 2 **C)** 5 **D)** 3

5. Serial binary adder is a _____circuit [ ]
A)combinational **B)** sequential **C)** A or B **D)** None

6. A 4 bit parallel adder is designed using _____number of full adders [ ]
A) 2 **B)** 4 **C)** 5 **D)** 3

7. The logic expression for carry of half adder circuit is_____ [ ]
A) A'B **B)** AB **C)** AB' **D)** None

8. The logic expression for sum of half adder circuit is_____ [ ]
A) A'B **B)** A xor B **C)** AB' **D)** None

9. In a half subtractor circuit borrow expression is_____ [ ]
A) A'B **B)** AB **C)** AB' **D)** None

10. The logic expression for difference of half subtractor circuit is_____ [ ]
A) A xor B xor C **B)** B xor C **C)** A xor B **D)** None

11. The logic expression for sum of full adder circuit is_____ [ ]
A) A'BC **B)** A xor B xor C **C)** B xor C **D)** None

12. The logic expression for carry of full adder circuit is_____ [ ]
A) ABC **B)** A xor B xor C **C)** B xor C **D)** None

13. In a full subtractor circuit difference expression is_____ [ ]
A) A xor B xor C **B)** B xor C **C)** A xor C **D)** B xor C

14. In a full subtractor circuit borrow expression is_____ [ ]
A) A xor B xor C **B)** B xor C **C)** A xor C **D)** None

15. The full adder circuit is implemented using _____number of half adder circuits [ ]
A) 3 **B)** 1 **C)** 2 **D)** 4

16. The full subtractor circuit is implemented using _____number of half subtractor circuit [ ]
A) 3 **B)** 1 **C)** 2 **D)** 4

17. Complement of a bit in adder - subtractor circuit is [ ]
A)inverter **B)** XOR **C)** AND **D)**None

18. Carry look ahead adder reduces _____ [ ]
A)carry propagation time **B)** carry generation time **C)** sum generation time **D)** None

19. For an n-bit adder there are _____ gate levels for the carry to propagate from input to output [ ]

A)3n **B)** 4n **C)** 2n **D)** None

20. In carry look ahead adder C_{i+1}=_____ [ ]

A)$G_i+P_iC_i$ **B)** $G_i+P_{i+1}C_i$ **C)** $G_{i+1}+P_iC_i$ **D)**None

21. In magnitude comparison of A,B the output of a xor gate if they are equal is ---------
22. In magnitude comparison of A,B the output of a xnor gate if they are equal is --------
23. In magnitude comparison of A,B the output of a xor gate if they are unequal is --------
24. In magnitude comparison of A,B the output of a xnor gate if they are unequal is --------
25. Minimum number of half adders required for 2 bit multiplier is ----------
26. If A=1010 and B=0100 .Then output of a 4 bit parallel adder is_____
27. A decoderwith n input provides _____minterms at the output.
28. A encoder has --------number of inputs and --------number of outputs
29. The number of output lines in 1X4 demultiplexer is_____
30. The number of AND gates required to implement 3 X 8 decoder along with 3 not gates is__
31. To implement full adder ---------size decoder is required
32. A 4X16 decoder can be designed using _____ number of 3x8 decoders
33. An octal to binary encoder is implemented using 3_____ gates
34. The number of select inputs in 32X1 multiplexer is_____
35. The binary variable (A=**B)** is equal to _____ only if all pairs of digits of the two numbers are equal
36. In a 4X2 priority encoder with D3 with highest priority the output XY for input 1111 is_____
37. The decimal adder is also known as _____adder
38. Multiplexer is also called as
39. Demultiplexer is also called as
40. The decimal adder is also known as _____adder
41. The number of 4X1 multiplexers required to design 16X1 multiplexer is ____
42. A 2bit multiplier can design using minimum of
43. A ripple counter's speed is limited by the propagation delay of -------
44. To operate correctly, starting a ring counter requires --------

UNIT-4

1. The output Y of a 2-bit comparator is logic 1 whenever the 2 bit input A is greater than the 2 bit input B. The number of combinations for which the output is logic 1, is

A. 4 **B**. 6 **C**. 8 **D**. 10

GATE 2012 [ ]

2. A switch-tail ring counter is made by using a single D flip flop. The resulting circuit is a

GATE 1995 [ ]

A. SR flip flop **B**. JK flip flop **C**. D flip flop **D**. T flip flop

3. An SR latch is a **GATE 1995 [ ]**

A. Combinational circuit **B**. Synchronous sequential circuit

C. One bit memory element **D**. One clock delay element

4. The present output Q_n of an edge triggered JK flip-flop is logic '0'. If j = 1, then Q_{n+1} is
GATE 2005 [ ]
A. Cannot be determined **B**. Will be logic '0'

C. Will be logic '1' **D**. Will race around

5. A 4 bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each flip-flop is 50 nsec, the maximum clock frequency that can be used is equal to ____.
GATE 1990 [ ]

A. 20 MHz **B**. 10 MHz **C**. 5 MHz **D**. 4 MHz

6. Synchronous counters are _____ than the ripple counters. **GATE1994** **[ ]**
A. Slower **B**. Faster **C**. Moderate **D**. None

7. A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then **GATE 2003** **[ ]**
A. R = 10 ns, S = 40 ns **B**. R = 40 ns, S = 10 ns

C. R = 10 ns, S = 30 ns **D**. R = 30 ns, S = 10 ns

8. In sequential Circuits, the output variable depends on _____of the input variable. []
A. Present State **B**. Past State **C**. Both **D**. None

9. The Serial adder is a _____Circuit. []
A. Combinational **B**. Sequential **C**. Both **D**. None

10. The outputs of any sequential circuit are always _____to each other.
A. Complementary **B**. Independent **C**. Pearson **D**. None

11. In S-R latch, if S=R=1, the present state of the latch is. [ ]
A. 1 **B**. 0 **C**. Undetermined **D**. None

12. The D- latch sometimes called as _____ Latch. [ ]
A. Flipflop **B**. Buffer **C**. Transparent **D**. None

13. _____and_____are building blocks of Sequential Circuits. [ ]
A. Flipflop **B**. Latches **C**. Both **D**. None

14. In _____Triggering, the output of Flipflop responds to the input changes only when its enable input is Low. [ ]
A. Negative Level **B**. Positive Level **C**. Edge **D**. None

15. If S=0, R=1 and CP = 0 to which Q_n= 0\1, the S-R Flipflop will be in __State. [ ]
A. No change **B**. 1 **C**. 0 **D**. Undetermined

16. The Basic building block of D- flipflop is ____Flipflop. [ ]
A. J-K **B**. Master-Slave **C**. S-R **D**. None

17. The output $Q_{n+1}$is delayed by one clock period for an D- Flipflop to which it is called as ____Flipflop. []
A. J-K **B**. Master-Slave **C**.S-R **D**. Delay

18. For the Inputs J=0, K=0, the output Q will be in ____state. []
A. Reset **B**. Undertermined **C**.Nochange **D**. Delay

19. In JK flipflop, when J = K = 1, the output the Flipflop will be in ____state. []
A. Reset **B**. Undertermined **C**. Toggling **D**. Delay

20. _____will not be an clock input of the Master-slave Flipflop. [ ]
A. Edge Triggered **B**. Level Triggered **C**.Both **D**. None

21. The ____ Flipflop is a modification of JK Flipflop.
22. If P = C = 0, the flipflop will be in _____ State.
23. For Moore Sequential Circuit, the output depends on____ State.
24. The state reduction technique avoids _____states.
25. The Input and Output of a register can be controlled by connecting ____.
26. The _____ are used to transfer and storage of data in the registers.
27. The acronym of SIPO is_____.
28. The _____ register has capability of both shifts and parallel load.
29. The_____counters are simple in construction for more no. of states.
30. The Major limitation of Ripple counter is_____.

UNIT-5

This set of Digital Electronics/Circuits Multiple Choice Questions & Answers (MCQs) focuseson "Diode-Transistor Logic(DTL)

1. Diode–transistor logic (DTL) is the direct ancestor of _____
a) Register-transistor log b) Transistor–transistor logic
c) High threshold logic d) Emitter Coupled Logic
2. In DTL logic gating function is performed by _____
a) Diode b) Transistor c) Inductor d) CapacitoR
3. In DTL amplifying function is performed by _____
a) Diode b) Transistor c) Inductor d) Capacitor
4. How many stages a DTL consist of?
a) 2 b) 3 c) 4 d) 5
5. The full form of CTDL is _____
a) Complemented transistor diode logic b) Complemented transistor direct logic
c) Complementary transistor diode logic d) Complementary transistor direct logic
6. The DTL propagation delay is relatively _____
a) Large b) Small c) Moderate d) Negligible
7. The way to speed up DTL is to add an across intermediate resister is _____
a) Small "speed-up" capacitor b) Large "speed-up" capacitor
c) Small "speed-up" transistor d) Large " speed-up" transistor
8. The process to avoid saturating the switching transistor is performed by _____
a) Baker clamp b) James R. Biard c) Chris Brown d) Totem-Pole
9. A major advantage of DTL over the earlier resistor–transistor logic is the _____

a) Increased fan out b) Increased fan in c) Decreased fan out d) Decreased fan in
10. To increase fan-out of the gate in DTL _____
a) An additional capacitor may be used b) An additional resister may be used
c) An additional transistor and diode may be used d) Only an additional diode may be used---

XIII. WEBSITES:

1. **www.asic-world.com**
2. **www.nptel.ac.in**
3. **www.learnabout-electronics.org**

XIV . MOOCS SWAYAM NPTEL COURSE AS DIGITAL CIRCUITS

(onlinecourses.nptel.ac.in/noc18_ee33) – 12week course.

XV. JOURNALS:

INTERNATIONAL

1. International journal of Analog and Digital Electronics
2. International journal of Digital Electronics
3. International journal of Electronic Security and Digital Forensics

XVI. CASE STUDIES / SMALL PROJECTS:

1. Digital Fan speed regulator

2. Traffic controller

3. Adaptive lighting system for automobiles

4. Automatic LED emergency light.