ELECTRONIC DEVICES AND CIRCUITS (EC301PC)

COURSE PLANNER

I. COURSE OVERVIEW:

The course has been designed to introduce fundamental principles of Electronic Devices and Circuits. The students completing this course will understand basic Electronic Devices and Circuits, including semiconductor properties, operational amplifiers,. Finally, students will gain experience in with the design of analog amplifiers, power supplies and logic devices.

II. PREREQUISITS:

1. Semiconductor Physics
2. Basic Electronics

III. COURSE OBJECTIVES:

1.	To introduce components such as diodes, BJTs and FETs.
2.	To know the applications of components.
3.	To know the switching characteristics of components.
4.	To give understanding of various types of amplifier circuits.

IV. COURSE OUTCOMES:

S.No.	Description	Bloom's Taxonomy Level
1.	Know the characteristics of various components.	Knowledge, Understand (Level1, Level2)
2.	Understand the utilization of components.	Apply, Create (Level 3, Level 6)
3.	Understand the biasing techniques.	Knowledge, Understand (Level1, Level2)
4.	Design and analyze small signal amplifier circuits.	Analyze (Level 4)

V. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (PO)		Level	Proficiency assessed by
PO1	**Engineering Knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.	3	Assignments
PO2	**Problem Analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	2	Examples
PO3	**Design/ Development of Solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Assignments, Exercises
PO4	**Conduct Investigations of Complex Problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	-	-
PO5	**Modern Tool Usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	-	-
PO6	**The Engineer and Society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.	-	-
PO7	**Environment and Sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	-	-
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	-	-
PO9	**Individual and Team Work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	1	Oral Discussions
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	2	Document Preparation, Presentation
PO11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team,	2	Assignments

Program Outcomes (PO)		Level	Proficiency assessed by
	to manage projects and in multidisciplinary environments.		
PO12	**Life-Long Learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	2	Assignments

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VI. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	2	Lectures, Assignments
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	1	Tutorials
PSO 3	**Successful Career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	-	-

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

VII. SYLLABUS:

UNIT - I:

Diode and Applications: Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances, Diode Applications: Switch-Switching times. Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive and Inductive Filters, Clippers-Clipping at two independent levels, Clamper-Clamping Circuit Theorem, Clamping Operation, Types of Clampers.

UNIT - II:

Bipolar Junction Transistor (BJT): Principle of Operation, Common Emitter, Common Base and Common Collector Configurations, Transistor as a switch, switching times,

Transistor Biasing and Stabilization - Operating point, DC & AC load lines, Biasing - Fixed Bias, Self Bias, Bias Stability, Bias Compensation using Diodes.

UNIT - III:

Junction Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, Biasing of FET, FET as Voltage Variable Resistor.

Special Purpose Devices: Zener Diode **-** Characteristics, Voltage Regulator. Principle of Operation - SCR, Tunnel diode, UJT, Varactor Diode.

UNIT – IV:

Analysis and Design of Small Signal Low Frequency BJT Amplifiers: Transistor Hybrid model, Determination of h-parameters from transistor characteristics, Typical values of h-parameters in CE, CB and CC configurations, Transistor amplifying action, Analysis of CE, CC, CB Amplifiers and CE Amplifier with emitter resistance, low frequency response of BJT Amplifiers, effect of coupling and bypass capacitors on CE Amplifier.

UNIT – V:

FET Amplifiers: Small Signal Model**,** Analysis of JFET Amplifiers, Analysis of CS, CD, CG JFET Amplifiers. MOSFET Characteristics in Enhancement and Depletion mode, Basic Concepts of MOS Amplifiers.

TEXT BOOKS:

1. Electronic Devices and Circuits- Jacob Millman, McGraw Hill Education
2. Electronic Devices and Circuits theory– Robert L. Boylestead, Louis Nashelsky, 11th Edition, 2009, Pearson**.**

REFERENCE BOOKS:

1. The Art of Electronics, Horowitz, 3rd Edition Cambridge University Press
2. Electronic Devices and Circuits, David A. Bell – 5th Edition, Oxford.
3. Pulse, Digital and Switching Waveforms –J. Millman, H. Taub and Mothiki S. Prakash Rao, 2Ed., 2008, Mc Graw Hill.

NPTEL Web Course: https://nptel.ac.in/courses/117108107/9, https://nptel.ac.in/courses/117103063

NPTEL Video Course: https://nptel.ac.in/courses/117108107/9, https://nptel.ac.in/courses/117103063

GATE SYLLABUS:

Energy bands in intrinsic and extrinsic silicon; Carrier transport current, drift current, mobility and resistivity; Generation and recombination of carriers; Poisson and continuity equations; P-N junction, Zener diode, BJT, MOS capacitor, MOSFET, LED etc.

ESE/ IES SYLLABUS:

Basics of semiconductors; Diode/Transistor basics and characteristics; Diodes for different uses; Junction & Field Effect Transistors (BJTs, JFETs, MOSFETs); Transistor amplifiers of

different types, oscillators and other circuits; Basics of Integrated Circuits (ICs); Bipolar, MOS and CMOS ICs; Basics of linear ICs, operational amplifiers and their applications-linear/non-linear; Optical sources/detectors; Basics of Opto electronics and its applications.

VIII. COURSE PLAN (WEEK-WISE):

Session	Week	Unit	Topic to be covered	Link for PPT	Link for small project / Numerical (if any)	Course Learning Outcomes	Teaching Methodology	Reference
1	1	1	**Unit-I**: Introduction	https://drive.google.com/drive/u/1/folders/1GJBqcyThwMfIP7dKGJ8xj7ypdMsSEVSU	https://drive.google.com/drive/u/1/folders/1GJBqcyThwMfIP7dKGJ8xj7ypdMsSEVSU	**Know** the physics of P-N junction.	Chalk and Talk	**T1, T2**
2			Diode - Static and Dynamic resistances			**Understand** the Diode - Static and Dynamic resistances	Chalk and Talk	**T1, T2**
3			P-N junction Equivalent circuit			**Understand** the diode Equivalent circuit	Chalk and Talk	**T1, T2**
4			Load line Analysis			**Understand** the Load line analysis	Chalk and Talk	**T1, T2**
5	2		Effect of temperature, diode resistance			**Understand** the temperature effects and diode resistance	Chalk and Talk	**T1, T2**
6			Diffusion Capacitance, *****. Drift Capacitance***			**Know** about drift and diffusion capacitances.	Chalk and Talk	**T1, T2**
7			Diode switching times			**Understand** diode switching times.	Discussion	**T1, T2**

8			Rectifier - Half Wave Rectifier			**Understand** the concept of Rectifier - Half Wave Rectifier	Chalk and Talk	**T1, T2**
9	3		Full Wave Rectifier, Bridge Rectifier			**Understand** the operation, characteristics and applications of Full Wave Rectifier, Bridge Rectifier	Chalk and Talk	**T1, T2**
10			Rectifiers with Capacitive and Inductive Filters			**Understand** the operation, characteristics and applications of Rectifiers with Capacitive and Inductive Filters.	Chalk and Talk	**T1, T2**
11			Rectifiers with Capacitive and Inductive Filters			**Understand** the operation, characteristics and applications of Rectifiers with Capacitive and Inductive Filters.	Chalk and Talk, PPTs	**T1, T2**
12			Clippers-Clipping at two independent levels			**Understand** how the diode acts as Clippers-Clipping at two independent levels	Chalk and Talk, PPTs	**T1, T2**
13	4		Clamper-Clamping Circuit Theorem			**Understand** how the diode acts as Clamper-Clamping Circuit Theorem	Chalk and Talk, PPTs	**T1, T2**

14			Clamping Operation, Types of Clampers.			**Understand** the general conditions for Clamping Operation, Types of Clampers..	Chalk and Talk, PPTs	**T1, T2**
15			Clamping Operation, Types of Clampers.			**Understand** the general conditions for Clamping Operation, Types of Clampers..	Chalk and Talk, PPTs	
16			**Mock Test-I**					
17	5	**2**	**<u>Unit-II</u>**: Transistor characteristics: The junction transistor			**Understand** the basics of transistors.	Chalk and Talk, PPTs	**T1, T2**
18			Principle of Operation			**Study** the operation of transistor	Chalk and Talk, PPTs	**T1, T2**
19			Common Emitter Configurations			**Study** the characteristics of CE configurations.	Chalk and Talk, PPTs	**T1, T2**
20			Common Base Configurations			**Study** the characteristics of CB configurations.	Chalk and Talk, PPTs	**T1, T2**
21	6		Bridge Class					
22			Common Collector configurations			**Study** the characteristics of CC configurations.	Chalk and Talk	**T1, T2**

23			Transistor as a switch			**Understand** the concept of Transistor as a switch	PPTs, discussions	**T1, T2**
24			switching times			**Study** about switching times.	Chalk and Talk	**T1, T2**
25	7		Transistor Biasing			**Explain** the operation of Transistor Biasing.	Chalk and Talk	**T1, T2, R1**
26			Stabilization			**Explain** the operation of Stabilization	Chalk and Talk, PPTs	**T1, T2, R1**
27			Bridge Class					
28			Operating point, DC & AC load lines			**Understand** the operation of Operating point, DC & AC load lines.	Chalk and Talk	**T1, T2**
29	8		Biasing - Fixed Bias, Bias Stability			Biasing - Fixed Bias, Bias Stability	Chalk and Talk	**T1, T2**
30		3	Self Bias, Bias Stability			**Understand** the operation, Self Bias, Bias Stability	Chalk and Talk, PPTs	**T1, T2**
31			Bias Compensation using Diodes.			**Understand** the operation, Bias Compensation using Diodes.	Chalk and Talk, PPTs	**T1, T2**
32			Bridge Class					

33	9		**<u>Unit-III</u>**: **JFET** Construction, Principle of Operation			**Understand** the operation of **JFET** Construction, Principle of Operation	Chalk and Talk, PPTs	**T1, T2**
34			Pinch-Off Voltage, Volt-Ampere Characteristic			**Understand** the Pinch-Off Voltage, Volt-Ampere Characteristic	Chalk and Talk, PPTs	**T1, T2**
35			Comparison of BJT and FET			**Understand** Comparison of BJT and FET	Chalk and Talk, PPTs	**T1, T2**
36				***I Mid Examinations (Week 9)***				
37	10	**3**	Biasing of FET	https://drive.google.com/drive/u/1/folders/1GJBqcyThwMfIP7dKGJ8xi7ypdMsSEVSU	https://drive.google.com/drive/u/1/folders/1GJBqcyThwMfIP7dKGJ8xi7ypdMsSEVSU	**Understand** the Biasing of FET	Chalk and Talk, PPTs	**T1, T2**
38			FET as Voltage Variable Resistor			**Understand** the FET as Voltage Variable Resistor.	Chalk and Talk, PPTs	**T1, T2**
39			Zener Diode – Characteristics			**Understand** the Zener Diode - Characteristics	Chalk and Talk, PPTs	**T1, T2**
40			Voltage Regulator			**Understand** the Voltage Regulator	Chalk and Talk, PPTs	**T1, T2**
41	11		Bridge Class					
42		**4**	Principle of Operation – SCR			**Understand** the Principle of Operation - SCR	Chalk and Talk, PPTs	**T1, T2**

43			Tunnel diode			**Understand** the Tunnel diode **Understand** the UJT	Chalk and Talk, PPTs	**T1, T2**
44			UJT				Chalk and Talk, PPTs	**T1, T2**
45			Bridge Class					
46			Varactor Diode.			**Understand** the Varactor Diode.	Chalk and Talk, PPTs	**T1, T2**
47	12		**UNIT – IV** Analysis and Design of Small Signal Low Frequency BJT Amplifiers:			**Analysis and Design** of Small Signal Low Frequency BJT Amplifiers:	Chalk and Talk, PPTs	**T1, T2**
48			Transistor Hybrid model				Chalk and Talk, PPTs	**T1, T2**
49	13		Determination of h-parameters from transistor characteristics			**Design** Determination of h-parameters from transistor characteristics	Chalk and Talk, PPTs	**T1, T2**
50			Typical values of h- parameters in CE configurations			**Understand** Typical values of h-parameters in CE configurations	Chalk and Talk, PPTs	**T1, T2**

51			Typical values of h- parameters in CBconfigurations			**Understand** Typical values of h-parameters in CB configurations	Chalk and Talk, PPTs	**T1, T2**
52			Bridge Class					
53	14		Typical values of h- parameters in CC configurations			**Understand** Typical values of h-parameters in CC configurations	Chalk and Talk, PPTs	**T1, T2**
54			Transistor amplifying action				Chalk and Talk, PPTs	**T1, T2**
55			Analysis of CE Amplifiers			**Analyze** the design of Analysis of CE,CB,CC Amplifiers	Chalk and Talk, PPTs	**T1, T2**
56			Analysis of CB Amplifiers					
57	16		Analysis of CC Amplifiers					
58			Bridge Class					
59		**5**	CE Amplifier with emitter resistance			**Analyze** the design of Analysis of CE Amplifier with emitter resistance	Chalk and Talk, PPTs	**T1, T2**

60			low frequency response of BJT Amplifiers			**Analyze** the design of Analysis of low frequency response of BJT Amplifiers	Chalk and Talk, PPTs	**T1, T2**
61			effect of coupling and bypass capacitors on CE Amplifier.			**Analyze** the design of Analysis of effect of coupling and bypass capacitors on CE Amplifier.	Chalk and Talk, PPTs	**T1, T2**
62	17		**UNIT – V FET Amplifiers,** JFET Small Signal Model, Analysis of JFET Amplifiers			**Analyze** the design of Analysis of JFET Small Signal Model	Chalk and Talk, PPTs	**T1, T2**
63			Analysis of CS,CG,CD JFET Amplifiers			**Analyze** the design of CS CG,CD JFET Amplifiers		
64			Analysis of CS,CG,CD JFET Amplifiers			**Analyze** the design of CS CG,CD JFET Amplifiers	Chalk and Talk, PPTs	**T1, T2**
65	18		MOSFET Characteristics in Enhancement and Depletion mode			**Analyze** the design of MOSFET Characteristics in Enhancement and Depletion mode	Chalk and Talk, PPTs	**T1, T2**
65			Basic Concepts of MOS Amplifiers.			**Analyze** the design of Basic Concepts of MOS Amplifiers.	PPTs	**T1, T2**
						II Mid Examinations (Week 18)		

IX. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course Outcomes	Program Outcomes												Program Specific Outcomes		
	PO 1	PO 2	PO3	PO 4	PO 5	PO 6	PO 7	PO8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CO1	3	2	3	-	-	-	-	-	1	-	-	2	2	1	-
CO2	3	2	2	-	-	-	-	-	-	-	-	2	2	-	-
CO3	3	2	3	-	-	-	-	-	-	2	3	-	-	-	-
CO4	3	2	2	-	-	-	-	-	-	2	1	-	2	-	-
Average	3	2	2.5	-	-	-	-	-	1	2	2	2	2	1	-
Average (Rounded)	3	2	3	-	-	-	-	-	1	2	2	2	2	1	-

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

X. JUSTIFICATIONS FOR CO-PO MAPPING:

Mapping	Low (1), Medium (2), High(3)	Justification
CO1-PO1	3	Students will be able to Students will be able to understand open circuited P-N junction.
CO1-PO2	2	Students will be able to understand how the diode acts as rectifier and study the characteristics of rectifiers.
CO1-PO3	3	Students will be able to understand the V-I characteristics of P-N junction.
CO1-PO9	1	Students will be able to understand the temperature effects and diode resistance
CO1-PO12	2	Know about drift and diffusion capacitances.
CO1-PSO1	2	Students will be able to understand diode switching times.
CO1-PSO2	2	Students will be able to understand the concept of breakdown in diodes and study the operation and characteristics of Zener diode.
CO2-PO1	3	Students will be able to understand the operation,

		characteristics and applications of tunnel diode
CO2-PO2	2	Students will be able to understand the operation, characteristics and applications of photo diode and LED.
CO2-PO3	2	To explain clipping circuits and comparators.
CO2-PO12	2	Students will be able to understand how the diode acts as rectifier and study the characteristics of rectifiers.
CO2-PSO1	2	Students will be able to understand the general conditions for filters and study the rectifier with capacitor filter.
CO3-PO1	3	To study the operation of transistor as an amplifier.
CO3-PO2	2	To study the characteristics of CB,CE,CC configurations.
CO3-PO3	3	Compare various configurations of transistors.
CO3-PO10	2	Understand the concept of operating point and purpose of biasing.
CO3-PO11	3	Study about bias compensation, thermal runaway and stability.
CO4-PO1	3	Explain the operation of transistor at low frequencies.
CO4-PO2	2	Explain the operation of CE amplifier, study its frequency response and gain bandwidth product.
CO4-PO3	2	Understand the operation of emitter follower.
CO4-PO10	2	Explain the operation of RC coupled two cascaded CE and multistage CE amplifiers.
CO4-PO11	1	Students will be able to understand the operation, V-I characteristics of JFET.
CO4-PSO1	2	Students will be able to understand the operation, V-I characteristics of MOSFFET.

XI. QUESTION BANK (JNTUH) :

UNIT - I

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Explain the formation of PN junction diode.	Remember	1
2.	Discuss the operation of PN junction diode as rectifier.	Understand	1
3.	Define biasing. Briefly describe the operation of PN diode under forward and reverse bias conditions.	Understand	1
4.	Sketch the V-I characteristics of p-n junction diode for forward bias voltages. Distinguish between the incremental resistance and the apparent resistance of the diode?	Evaluation	1
5.	Explain the temperature dependence of VI characteristics of PN diode?	Comprehension	1
6.	Derive an expression for total diode current starting from Boltzmann relationship in terms of the applied voltage?	Knowledge	1
7.	Explain the V-I characteristics of Zener diode and distinguish between Avalanche and Zener Break downs?	Understand	1
8.	Explain the concept of diode capacitance. Derive expression for transition capacitance?	Understand	1
9.	Define depletion region at p-n junction? What is the effect of forward and reverse biasing of p-n junction on the depletion region? Explain with necessary diagrams?	Remember	1
10.	Explain the tunneling phenomenon. Explain the characteristics of tunnel diode with the help of necessary energy band diagrams?	Understand	1
11.	What is the photo diode? Explain its principle of operation and applications in detail?	Remember	1
12.	Explain the construction and working of LED?	Understand	1
13.	Discuss the applications of diode as clipper circuits.	Remember	1
14.	Briefly explain the operation of a comparator.	Remember	1
15.	Draw the block diagram of a regulated power supply and explain its operation?	Understand	1
16.	Draw the circuit of a half-wave-rectifier and find out the ripple factor, % regulation? Efficiency and PIV?	Analyze	1
17.	Draw the circuit of bridge rectifier and explain its operation with the help of input and output waveforms?	Analyze	1
18.	With suitable diagrams, explain the working of centre-tapped full wave rectifier. Derive expressions for V_{DC}, I_{DC}, V_{rms} and I_{rms} for it?	Understand	1

19.	Explain the relative merits and demerits of all the rectifiers?	Understand	1
20.	Mention the need for filter circuits in rectifiers. Explain the working of capacitor filter.	Understand	1

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Define Electronics?	Remember	1
2.	Explain about forward bias of diode?	Understand	1
3.	Explain about reverse bias of diode?	Understand	1
4.	Write the applications of diode?	Comprehension	1
5.	Draw the V-I characteristics of diode?	Comprehension	1
6.	List the differences between ideal diode and practical diode?	Remember	1
7.	Define diffusion capacitance?	Knowledge	1
8.	Define transition capacitance?	Remember	1
9.	Define static resistance?	Remember	1
10.	Define dynamic resistance	Remember	1
	Write the equation of diode current	Remember	1
12.	Define cut-in voltage?	Remember	1
13.	Write the differences between avalanche and zener breakdown mechanisms?	Knowledge	1
14.	Define zener breakdown mechanism?	Remember	1
15.	Define depletion region?	Remember	1
16.	Explain the temperature dependence of VI characteristics of PN diode?	Understand	1
17.	Define doping?	Remember	1

18.	Explain about extrinsic semiconductor	Understand	1
19.	Explain about unbiased PN junction?	Understand	1
20.	Write down the expression for diode current?	Knowledge	1
21.	Define drift current?	Remember	1
22.	List the applications of Zener diode?	Analyze	1
23.	Define forbidden energy gap?	Remember	1
24.	With appropriate circuit diagram explain the DC load line analysis of semiconductor diode?	Analyze	1
25.	Define Peak Inverse voltage of a diode?	Remember	1
26.	What is the principle of operation of photodiode?	Knowledge	1
27.	Give the principle of operation of Light Emitting Diode?	Analyze	1
28.	Define diffusion current?	Remember	1
29.	List the applications of LED.	Analyze	1
30.	Define photodiode?	Remember	1

UNIT - II

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	With a neat diagram explain the various current components in an NPN bipolar junction transistor & hence derive general equation for collector current, I_C?	Understand	2
2.	Define Early-effect; explain why it is called as base-width modulation? Discuss its consequences in transistors in detail?	Remember	2
3.	How transistor acts as an amplifier?	Remember	2
4.	Draw the input and output characteristics of a transistor in common emitter configurations?	Comprehension	2
5.	Draw the input and output characteristics of a transistor in common base configurations?	Evaluate	2
6.	Draw the input and output characteristic of a transistor in common collector configurations?	Comprehension	2

7.	Explain the constructional details of Bipolar Junction Transistor?	Understand	2
8.	Derive the relation among α, β and γ?	Evaluation	2
9.	What is thermal runaway in transistors? Obtain the condition for thermal stability in transistors?	Remember	2
10.	Analyze general transistor amplifier circuit using h parameter model. Derive the expressions for A_I, A_V, R_i, R_o, A_{Is}, A_{Vs}.	Analyze	2
11.	Draw the circuit of an emitter follower, and derive the expressions for A_I, A_V, R_i, R_o in terms of CE parameters.	Remember	2
12.	Write the analysis of a CE amplifier circuit using h parameters. Derive the expressions for A_I, A_V, R_i, R_o, A_{Is}, A_{Vs}.	Analyze	2
13.	Define h-parameter of a transistor in a small signal amplifier. What are the benefits of h-parameters?	Remember	2
14.	Compare the different types of coupling methods used in multistage amplifiers.	Remember	2
15.	Sketch two RC-coupled CE transistor stages. Show the middle and low frequency model for one stage. Write the expressions for current gains.	Remember	2
16.	Explain about different methods of Inter stage coupling in amplifiers. When two stages of identical amplifiers are cascaded, obtain the expressions for overall voltage gain, current gain and power gain.	Understand	2

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	What is meant by operating point Q?	Comprehension	2
2.	Draw the symbols of NPN and PNP transistor?	Comprehension	2
3.	Explain the operation of BJT and its types?	Understand	2
4.	Explain the breakdown in transistor?	Understand	2
5.	Explain the transistor switching times?	Understand	2
6.	Define Transistor current?	Remember	2
7.	Define early effect or base width modulation?	Remember	2
8.	Explain about transistor amplifier?	Understand	2
9.	Define current amplification factor?	Remember	2

10.	When does a transistor act as a switch?	Comprehension	2
11.	Explain about the various regions in a transistor?	Understand	2
12.	Draw the small signal model of a CE configuration?	Knowledge	2
13.	Draw the output characteristics of NPN transistor in CE configuration?	Comprehension	2
14.	Define h_{ie} and h_{fe} in CE configuration?	Remember	2
15.	Define h_{oe} and h_{re} in CB configuration?	Remember	2
16.	Define saturation region?	Remember	2
17.	Write the relation between I_C, β, I_B and I_{CBO} in a BJT?	Knowledge	2
18.	Define cutoff region?	Remember	2
19.	Define active region?	Remember	2
20.	Describes the various current components in a BJT?	Knowledge	2
21.	Define amplifier?	Remember	2
22.	Draw the hybrid model of a CB configuration?	Knowledge	2
23.	List the classification of amplifiers.	Remember	2
24.	List the classification of amplifiers based on frequency of operation	Remember	2
25.	Define various hybrid parameters.	Remember	2
26.	Draw the hybrid equivalent model of CE Amplifier	Understand	2
27.	In a multistage amplifier, what is the coupling method required to amplify dc signals?	Remember	2
28.	Write the expression for lower 3 – dB frequency of an n – stage amplifier with non – interacting stages.	Remember	2
29.	Two stages of amplifier are connected in cascade. If the first stage has a decibel gain of 40 and second stage has an absolute gain of 20 then what is the overall gain in decibels.	Evaluate	2
30.	Why the overall gain of multistage amplifier is less than the product of gains of individual stages.	Understand	2
31.	What are the main characteristics of a Darlington amplifier?	Understand	2
32.	Why direct coupling is not suitable for amplification of high frequency	Understand	2

UNIT - III

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Explain the operation of FET with its characteristics and explain the different regions in transfer characteristics?	Comprehension	2
2.	Define pinch-off voltage and trans conductance in field effect transistors?	Comprehension	2
3.	With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on the characteristics?	Application	2
4.	Explain how a FET can be made to act as a switch?	Knowledge	2
5.	Bring out the differences between BJT and FET. Compare the three configurations of JFET amplifiers?	Knowledge	2
6.	Create a relation between the three JFET parameters, μ, r_d and g_m?	Creating	2
7.	How a FET can be used as a voltage variable Resistance (VVR)?	Remember	2
8.	Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?	Understand	2
9.	Sketch the drain characteristics of MOSFET for different values of VGS& mark different regions of operation.	Comprehension	2
10.	Explain the principle of CS amplifier with the help of circuit diagram. Derive the expressions for AV, input impedance and output Impedance?	Understand	2
11.	Discuss the high frequency response of CD Configuration?	Knowledge	2
12.	Draw the small-signal model of common drain FET amplifier. Derive expressions for voltage gain and output resistance?	Analyze	2

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Write the expressions for mid-frequency gain of a FET Common Source?	Knowledge	2
2.	Discuss the high frequency response of CD Configuration?	Knowledge	2
3.	What is the effect of external source resistance on the voltage gain of a common source amplifier? Explain with necessary derivations?	Remember	2
4.	Draw the small-signal model of common drain FET	Analyze	2

	amplifier. Derive expressions for voltage gain and output resistance?		
5.	Draw the small-signal model of common source FET amplifier.	Analyze	2
6.	Why FET is called a voltage operated device?	Evaluation	2
7.	List the important features of FET?	Knowledge	2
8.	Write short notes on millers theorem?	Knowledge	2
9.	Give the classifications of FETs and their application areas?	Knowledge	2
10.	Define pinch off voltage?	Comprehension	2
1.	Draw the structure of an n-channel JFET?	Knowledge	2
12.	Define rd and Gm?	Remember	2
13.	Draw the static characteristics curves of an n-channel JFET?	Comprehension	2
14.	Draw the drain characteristics of depletion type MOFET?	Knowledge	2
15.	Draw the small signal model of JFET?	Knowledge	2
16.	Draw the transfer characteristics for P-channel JFET?	Comprehension	2
17.	Draw the Drain V-I characteristics for p-channel JFET?	Knowledge	2
18.	Explain about ohmic and saturation regions?	Understand	2
19.	Draw the drain characteristics of an n-channel enhancement type MOSFET?	Knowledge	2
20.	Write the expressions for mid-frequency gain of a FET Common Source?	Knowledge	2

UNIT - IV

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Draw the circuit diagram & small signal equivalent of CB amplifier using accurate h-parameter model. Derive	Application	3

	expressions for A_V, A_I, R_i and R_0?		
2.	Draw the circuit diagram of CC amplifier using hybrid parameters and derive expressions for A_I, A_V, R_i, R_O?	Application	3
3.	What are the compensation techniques used for V_{BE} and I_{CO}. Explain with help of suitable circuits?	Remember	3
4.	Define the stability factors with respect to the changes in I_{CO}, V_{BE} and β. Why is the stability with respect to changes in V_{CE} not considered?	Remember	3
5.	Justify statement "Potential divider bias is the most commonly used biasing method" for BJT circuits. Explain how bias compensation can be done in such biasing through diodes?	Evaluate	3
6.	Determine the significance of operating point, DC and AC load lines to ensure active region operation of a BJT in CE amplifier application?	Evaluate	3
7.	A bipolar junction transistor with h_{ie} = 1100Ω, h_{fe} = 50, $h_{re} = 2.4x10^{-4}$, h_{oe} = 25 μA/V, is to drive a load of 1KΩ in CB amplifier arrangement. Estimate A_V, A_I, R_i& R_0?	Evaluate	3
8.	Design a fixed bias circuit using silicon transistor, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50?	Evaluate	3
9.	Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β = 50?	Evaluate	3
10.	Design a self bias circuit for the following specifications: V_{CC} = 12 V; V_{CE} = 2V; I_C = 4mA; h_{fe} = 80. Assume any other design required. Draw the designed circuit.	Evaluating parameters	3

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Which biasing method provides more stabilization amongst the three types of biasing methods?	Knowledge	3
2.	Compare the advantages and disadvantages of biasing schemes?	Understand	3
3.	Draw the circuit diagram of a collector to base bias circuit of CE amplifier?	Knowledge	3

4.	Write down advantages of fixed bias circuity?	Understand	3
5.	Draw the circuit diagram of a fixed bias circuit of CE amplifier?	Understand	3
6.	Draw a circuit employing a sensistor compensation?	Understand	3
7.	Write down disadvantages of fixed bias circuit?	Understand	3
8.	Define thermal runaway?	Understand	3
9.	Define thermal resistance?	Understand	3
10.	Define stability factors s' and s''?	Understand	3

UNIT - V

Long Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Write short notes on millers theorem?	Understand	4
2.	Give the classifications of FETs and their application areas?	Understand	4
3.	Define pinch off voltage?	Understand	4
4.	Draw the structure of an n-channel JFET?	Knowledge	4
5.	Define rd and Gm?	Understand	4
6.	Draw the static characteristics curves of an n-channel JFET?	Understand	4
7.	Draw the drain characteristics of depletion type MOFET?	Understand	4
8.	Draw the small signal model of JFET?	Understand	4
9.	Draw the transfer characteristics for P-channel JFET?	Understand	4
10.	Draw the Drain V_I characteristics for p-channel JFET?	Understand	4

Short Answer Questions:

S.No.	Question	Blooms Taxonomy Level	Course Outcome
1.	Draw the small-signal model of common gate FET amplifier. Derive expressions for voltage gain and output resistance?	Apply	4

2.	List any four merits of MOSFET to show that they are more suitable than JFETS in Integrated circuits?	Understand	4
3.	Compare enhancement and depletion modes of a MOSFET with the help of its characteristics and construction?	Apply	4
4.	With a neat schematic, explain how amplification takes place in a common drain amplifier?	Knowledge	4
5.	The P-channel FET has a $\|I_{DS}\|$=-12mA, $\|V_p\|$=5V, V_{GS} is 1.6 V. Determine I_D ,G_m and G_{m0} ?	Evaluate	4
6.	Data sheet for a JFET indicates that I_{DS}=10mA and $V_{GS(off)}$= -4V. Determine the drain current for V_{GS}=0V, -1V and -4V.	Evaluate	4
7.	In an n-channel FET, the effective channel width is 3×10^{-4}cm and the donor impurity concentration is 10^{15} electrons/cm^3. Find the pinch-off voltage?	Evaluate	4
8.	A Common Source FET amplifier circuit with un-bypassed R_S has the following circuit parameters: R_d = 15K, R_S = 0.5K, R_g = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Calculate A_V, A_I, R_i and R_0?	Evaluate	4
9.	A Common Source FET amplifier circuit with un bypassed R_S has the following circuit parameters: R_d = 15K, R_S = 0.5K, R_g = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Determine A_V& R_O?	Evaluate	4
10.	A self biased p – channel JFET has a pinch – off voltage of V_P = 5 V and I_{DSS} = 12 mA. The supply voltage is 12 V. Determine the values of R_D and R_S so that I_D = 5 mA and V_{DS} = 6V?	Evaluate	4

OBJECTIVE QUESTIONS:

UNIT-I

1. The conventional current in a PN junction diode flows: [ ]
   (a) From positive to negative (b) From negative to positive
   (c) In the direction opposite to the electron flow. (d) Both (a) and (c) above
2. The cut in voltage (or knee voltage) of a silicon diode is [ ]
   (a) 0.2V (b) 0.6V (c) 0.8 V (d) 1.0V
3. When a diode is reverse biased, it is equivalent to [ ]
   (a) An OFF switch (b) an ON switch
   (c) A high resistance (d) none of the above
4. The resistance of a diode is equal to [ ]
   (a) Ohmic resistance of the P- and N- semiconductors (b) Junction resistance
   (c) Reverse resistance (d) Algebraic sum of (a) and (b) above
5. For a silicon diode, the value of the forward - bias voltage typically [ ]
   (a) Must be greater than 0.3V

(b) Must be greater than 0.7V
(c) Depends on the width of the depletion region
(d) Depends on the concentration of majority carriers

6. When forward biased, a diode [ ]
(a) Blocks current (b) conducts current
(c) Has a high resistance (d) drops a large voltage.

7. A PN junction diode's dynamic conductance is directly proportional to [ ]
(a) The applied voltage (b) the temperature
(c) The current (d) the thermal voltage

8. The forward region of a semiconductor diode characteristic curve is where diode appears as [ ]
(a) Constant current source (b) a capacitor
(c) An OFF switch (d) an ON switch

9. At room temperature of25 °C, the barrier potential for silicon is 0.7 V. lts value at 125° C is[]
(a) 0.5V (b) 0.3V (c) 0.9V (d) 0.7V

10. Junction breakdown of a PN junction occurs [ ]
(a) With forward bias (b) with reverse bias
(c) Because of manufacturing defect (d) None of these

11. Reverse saturation current in a silicon PN junction diode nearly doubles for every [ ]
(a) 2° C rise in temperature (b) 5° C rise in temperature
(c) 6° C rise in temperature (d) 10° C rise in temperature

12. The transition capacitance of a diode is 1nF and it can withstand a reverse potential of 400V. A capacitance of 2nF which can withstand a reverse potential of 1 kV is obtained by connecting [ ]
(a) two 1nF diodes in series
(b) six parallel branches with each branches comprising there 1nF diodes in series
(c) two 1nF diodes in series
(d) three parallel branches with each branch comprising 1nF diodes in series

13. A zener diode [ ]
(a) has a high forward-voltage rating
(b) has a sharp breakdown at low reverse voltage
(c) is useful as an amplifier
(d) has a negative resistance

14. A tunnel- diode is [ ]
(a) a very heavily-doped PN junction diode
(b) a high resistivity PN junction diode
(c) a slow switching device
(d) used with reverse bias

15. The light-emitting diode (LED) [ ]
(a) is usually made from silicon
(b) uses a reverse-biased junction
(c) gives a light output which increases with the increase in temperature
(d) depends on the recombination of holes and electrons

16. LED's do not require [ ]
    (a) heating (b) warm-up time
    (c) both (a) and (b) above (d) non of above
17. The sensitivity of a photodiode depends upon [ ]
    (a) light intensity and depletion region width
    (b) depletion region width and excess carrier life time
    (c) Excess carrier life time and forward bias current.
    (d) Forward bias current and light intensity.
18. LEDs are commonly fabricated from gallium compounds like gallium arsenide and gallium phosphide because they
    [ ]
    (a) are cheap (b) are easily available
    (c) emit more heat (d) emit more light.
19. A LED is basically a _____ P-N junction. [ ]
    (a) forward-biased (b) reverse-biased
    (c) lightly-doped (d) heavily-doped
20. As compared to a LED display, the distinct advantage of an LCD display is that it requires
    [ ]
    (a) No illumination (b) extremely-bias
    (c) No forward-bias (d) a solid crystal

UNIT-II

1. The "cut-in" voltage of a silicon small-signal transistor is [ ]
   (a) 0V (b) 0.2V (c) 0.5V (d) 0.8V
2. When the collector junction in transistors is biased in the reverse direction and the emitter junction in the forward direction, the transistor is said to be in the [ ]
   (a) Active region (b) cut-off region
   (c) Saturation region (d) none of them.
3. The transistor is said to be in saturation region when [ ]
   a. both collector and emitter junctions are forward biased
   b. both collector and emitter junctions are reversed biased
   c. emitter junction is forward biased, but the collector junction is reverse biased
   d. emitter junction is reverse biased, but the collector junction is forward biased
4. For a silicon transistor in the common emitter configuration the cut-off condition is achieved by applying a minimum reverse voltage across the emitter junction of the order of [ ]
   (a) 0V (b) 0.7 V (c) 1.5V (d) 5V
5. A transistor connected in common base configuration has [ ]
   I. a high input resistance and a low output resistance
   II. a low input resistance and high output resistance
   III. a low input resistance and a low output resistance
   IV. a high input resistance and a high output resistance
6. Which of the following is not a time varying quantity? [ ]
   (a) v_{ce} (b) V_{CE} (c) v_{CE} (d) V_{ce}
7. In the Ebbers-Model of a bipolar transistor, the parameter is the [ ]

(a) Forward transmission from emitter to collector
(b) Reverse transmission from collector to emitter
(c) Common base current gain
(d) Both (a) and (c) above

8. The value of trans-conductance of a bipolar transistor for a collector current of 1.5 mA is [ ]
(a) 0.05Ω (b) 0.05 x 10^3 Ω (c) 37.5 Ω (d) None of the above

9. The resistance $r_{bb'}$ in the low frequency hybrid-π model of a bipolar transistor represents [ ]

(a) Base spreading resistance A.C. resistance for forward biased emitter-base junction
(b) The effect of feedback between the emitter-base junction and collector-base junction due to Early effect
(c) None of the above

10. The capacitance C_e in the high frequency hybrid-π model of a bipolar transistor represents the [ ]
(a) Depletion region capacitance (b) Emitter diffusion capacitance
(c) Emitter-base junction capacitance (d) Sum of the (b) and (c) above

11. 11. For a common emitter amplifier having a small un bypassed emitter resistance (R_E) the input resistance is approximately equal to
[ ]
(a) R_E (b) h_{fe} (c) h_{fe} R_E (d) R_E /h_{fe}

12. The voltage gain of a common base amplifier is [ ]
(a) zero (b) less than unity (c) unity (d) greater than unity

13. For a common base transistor amplifier having input resistance (R_i) and output resistance (R_0), which of the following statements holds good
[ ]
(a) R_i is low, R_0 is high (b) R_i is high, R_0 is low
(c) R_i and R_0 are both medium (d) None of these

14. The current gain of an emitter follower is [ ]
(a) zero (b) greater than unity (c) less than unity (d) all of them

15. Which of the following transistor amplifiers has the highest voltage gain? [ ]
(a) common-base (b) common-collector
(c) common-emitter (d) none of them

16. In an ac amplifier, larger the internal resistance of the ac signal source [ ]
(a) Greater the overall voltage gain (b) greater the input impedance
(c) Smaller the current gain (d) smaller the circuit voltage gain.

17. The main use of an emitter follower is as [ ]
(a) power amplifier (b) impedance matching device
(c) low-input impedance circuit (d) follower of base signal.

18. An ideal amplifier is one which [ ]
(a) has infinite voltage gain (b) responds only to signal at its input terminals
(c) has positive feedback (d) gives uniform frequency response.

19. The voltage gain of a single-stage amplifier is increased when [ ]

(a) its ac load is decreased (b)resistance of signal source is increased
(c) emitter resistance R_E is increased. (d) as load resistance is increased.

20. When emitter bypass capacitor in a common-emitter amplifier is removed, its _____ is considerably reduced. [ ]
(a) input resistance (b) output load resistance
(c) emitter current (d) voltage gain

21. Unique features of a CC amplifier circuit is that it [ ]
(a) steps up the impedance level (b) does not increases signal voltage
(c) acts as an impedance matching device (d) all of the above.

22. The h-parameters are called hybrid parameters because they [ ]
(a) are different from y- and z - parameters.
(b) are mixed with other parameters
(c) apply to circuits contained in a box
(d) are defined by using both open-circuit and short-circuit terminations

23. Which of the following statement is not correct regarding the h-parameters of a transistor [ ]
(e) The values of h-parameters can be obtained from transistor characteristics.
(f) Their values depends upon the transistor configuration
(g) Their values depend on operating point
(h) They are four in number

24. Which of the following four h-parameters of a transistor has a greatest value [ ]
(a) h_i (b) h_r (c) h_0 (d) h_f

25. Which of the following four h-parameters of a transistor has a smallest value? [ ]
(a) h_i (b) h_r (c) h_0 (d) h_f

26. The typical value h_{ic} is [ ]
(a) l KΩ (b) 40 KΩ (c) 100KΩ (d) 2MΩ

27. The h-parameters of a transistor depend on its [ ]
(a) Configuration (b) operating point
(c) Temperature (d) all of the above

28. The output admittance h_0 of an ideal transistor connected is common-base configuration is _____ Siemens [ ]
(a) 0 (b) $\frac{1}{r}$ (c) $\frac{1}{\beta R_g}$ (d) -1

29. A transistor has h_{fe} = 100, h_{ie} = 5.2 KΩ, and r_{bb} = 0. At room temperature, V_T= 26 mV. The collector current, I_C will be [ ]
(a) 10 mA (b) 5 mA (c) l mA (d) 0.5 mA

UNIT-III

1. A field effect transistor (FET) operates on [ ]
(a) Majority carriers only (b) Minority carriers only
(c) Positively charged ions only

2. In JFET operating above pinch-off voltage, the [ ]
(a) Drain current remains practically constant
(b) Drain current starts decreasing
(c) Drain current increases rapidly
(d) Depletion region becomes smaller

3. The JFET is oftenly called square law device because its [ ]
   (a) Trans-conductance curve is parabolic
   (b) A.C. resistance from drain-to-source varies inversely as square of the drain current
   (c) Drain current varies as square of drain voltage for a fixed gate- to-source voltage
   (d) Reverse gate leakage current varies as a square of the reverse gate voltage
4. For the operation of depletion-type MOSFET, the gate voltage has to be [ ]
   (a) Low positive (b) High positive
   (c) High negative (d) Zero
5. The N-channel MOSFET devices are preferred more than P-channel's because [ ]
   (a)N-channel devices are faster than P-channel devices
   (b) N-channel devices consumes less power than P-channel devices
   (c)N-channel devices have higher packing density than P-channe1 devices
   (d) Both (a) and (c) above
6. As compared to N-channel MOS switch, the P-channel MOS switch has [ ]
   (a) Same ON resistance (b) Less ON resistance
   (a) More ON resistance (d) either (a) or (b)
7. Thermal runway is not possible in FET because as the temperature of the FET increases [ ]
   (a) the mobility decreases (b) the trans-conductance increases
   (c) the drain current increases (d) the mobility increases
8. Before illuminating a P-N junction photodiode, it has to be [ ]
   (a) Reverse-biased (b) forward-biased
   (c) Switched ON (d) switched OFF.
9. A LED emits visible light when its _____ [ ]
   (a) P-N junction is reverse-biased (b) depletion region widens
   (c) Holes and electrons recombine (d) P-N junction becomes hot.

10. In LED, light is emitted because [ ]
   (a) Recombination of charge carriers takes place
   (b) Diode gets heated up
   (c) Light falling on the diode gets amplified
   (d) Light gets reflected due to lens action.

UNIT-IV

1. The "cut-in" voltage of a silicon small-signal transistor is [ ]
   (a) 0V (b) 0.2V (c) 0.5V (d) 0.8V
2. When the collector junction in transistors is biased in the reverse direction and the emitter junction in the forward direction, the transistor is said to be in the [ ]
   (a) Active region (b) cut-off region
   (c) Saturation region (d) none of them.
3. The transistor is said to be in saturation region when [ ]
   a. both collector and emitter junctions are forward biased
   b. both collector and emitter junctions are reversed biased ·
   c. emitter junction is forward biased, but the collector junction is reverse biased
   d. emitter junction is reverse biased, but the collector junction is forward biased
4. For a silicon transistor in the common emitter configuration the cut-off condition is achieved by applying a minimum reverse voltage across the emitter junction of the order

of [ ]
(a) 0V (b) 0.7 V (c) 1.5V (d) 5V

5. A transistor connected in common base configuration has [ ]
   i. a high input resistance and a low output resistance
   ii. a low input resistance and high output resistance
   iii. a low input resistance and a low output resistance
   iv. a high input resistance and a high output resistance
6. In the Ebbers-Model of a bipolar transistor, the parameter is the [ ]
   a. Forward transmission from emitter to collector
   b. Reverse transmission from collector to emitter
   c. Common base current gain
   d. Both (a) and (c) above
7. The value of trans-conductance of a bipolar transistor for a collector current of 1.5 mA is [ ]
   (a) 0.05Ω (b) 0.05 x 103 Ω (c) 37.5 Ω (d) None
8. The resistance rbb' in the low frequency hybrid-π model of a bipolar transistor represents [ ]
   a. Base spreading resistance
   b. A.C. resistance for forward biased emitter-base junction
   c. The effect of feedback between the emitter-base junction and collector-base junction due to early effect
   d. None of the above
9. The capacitance Ce in the high frequency hybrid-π model of a bipolar transistor represents the [ ]
   (a) Depletion region capacitance (b) Emitter diffusion capacitance
   (c) Emitter-base junction capacitance (d) Sum of the (b) and (c) above
10. For a common emitter amplifier having a small un bypassed emitter resistance (RE) the input resistance is approximately equal to [ ]
    (a) RE (b) hfe (c) hfe RE (d) RE /hfe
11. The voltage gain of a common base amplifier is [ ]
    (a) zero (b) less than unity (c) unity (d) greater than unity
12. For a common base transistor amplifier having input resistance (Ri) and output resistance (R0), which of the following statements holds good [ ]
    (a) Ri is low, R0 is high (b) Ri is high, R0 is low
    (c) Ri and R0 are both medium (d) None of these
13. The current gain of an emitter follower is [ ]
    (a) zero (b) greater than unity (c) less than unity (d) all of them
14. Which of the following transistor amplifiers has the highest voltage gain? [ ]
    (a) common-base (b) common-collector
    (c) common-emitter (d) none of them
15. In an ac amplifier, larger the internal resistance of the ac signal source [ ]
    (a) Greater the overall voltage gain (b) greater the input impedance
    (c) Smaller the current gain (d) smaller the circuit voltage gain.

16. The main use of an emitter follower is as [ ]
    (a) power amplifier (b) impedance matching device
    (c) low-input impedance circuit (d) follower of base signal.
17. An ideal amplifier is one which [ ]
    (a) has infinite voltage gain (b) responds only to signal at its input terminals
    (c) has positive feedback (d) gives uniform frequency response.
18. The voltage gain of a single-stage amplifier is increased when [ ]
    (a) its ac load is decreased (b) resistance of signal source is increased
    (c) emitter resistance RE is increased. (d) as load resistance is increased.
19. When emitter bypass capacitor in a common-emitter amplifier is removed, its _____ is considerably reduced. [ ]
    (a) input resistance (b) output load resistance
    (c) emitter current (d) voltage gain

UNIT-V

1. Which of the following statement is not true in case of FET. [ ]
   (a) It has high input impedance (b) It is less noisy than bipolar transistor.
   (c) It has a large gain band width product (d) all of the above.
2. The JFET is a [ ]
   a) current controlled device with high input resistance
   b) voltage controlled device with high input resistance
   c) voltage controlled device with low input resistance
   d) current controlled device with low input resistance
3. The input impedance of a JFET is in the range of [ ]
   (a) above 2 MΩ (b) 200 to 400 KΩ (c) 20 to 40 KΩ (d) below 2 KΩ
4. FET is [ ]
   (a) current controlled device (b) voltage controlled device
   (c) resistance controlled device (d) reactance controlled device
5. In a FET, 10 volts reverse voltage is applied. If gate current is 0.1μA, the input resistance is
   [ ]
   (a) 1 MΩ (b) 10 MΩ (c) 100 MΩ (d) none of these
6. The best location for setting a Q-point on d.c. load line of an FET amplifier is at [ ]
   (a) saturation point (b) cut-off point
   (c) mid-point (d) none of the above
7. Which of the following bias methods provides a solid Q-point in JFET, amplifiers?
   [ ]
   (a) Gate bias (b) Self-bias
   (c) Voltage divider bias (d) Current source bias
8. Which of the following technique is used for biasing the enhancement type MOSFET`s?
   [ ]
   (a) Voltage divider bias (b) Collector feedback bias
   (c) Current source bias (d) Self-bias
9. The threshold voltage of an n-channel enhancement mode MOSFET is 0.5 V, when the device is biased at a gate voltage of 3V, pinch-of would occur at a drain voltage of

[ ]

(a) l.5 V (b) 2.5 V (c) 3.5V (d) 4.5V

10. The zero gate bias channel resistance of a junction field-effect transistor is 750 and the inch-off voltage is 3V. For a gate bias of 1.5 V and very low drain voltage, the device would behave as a resistance of [ ]
    (a) 320Ω (b) 816 Ω (c) l000 Ω (d) 1270 Ω
11. If properly biased, JFET with act as a [ ]
    (a) current controlled current source (b) voltage controlled voltage source
    (c) voltage controlled current source (d) current controlled voltage source
12. The best location for setting a Q-point on d.c. load line of an FET amplifier is at [ ]
    (a) Saturation point (b) cut-off point
    (c) Mid-point (d) none of these
13. Which of the following bias methods provides a solid Q-point in JFET amplifiers? [ ]
    (a) Gate bias (b) Self-bias
    (c) Voltage divider bias (d) Current source bias
14. Which of the following technique is used for biasing the enhancement type MOSFET? [ ]
    (a) Voltage divider bias (b) Collector feedback bias
    (c) Current source bias (d) Self-bias
15. The voltage gain of a common source JFET amplifier depends upon its [ ]
    (a) trans-conductance (gm) (b) amplification factor (μ)
    (c) external load resistance (RD) (d) both (a) and (c) above
16. A common gate amplifier has [ ]
    (a) high input resistance and high output resistance
    (b) low input resistance and high output resistance
    (c) low input resistance and low output resistance
    (d) high input resistance and low output resistance
17. A trans-conductance amplifier has [ ]
    (a) High input impedance and low output impedance
    (b) Low input impedance and high output impedance
    (c) High input and output impedances
    (d) Low input and output impedances
18. The threshold voltage of an-n-channel enhancement mode MOSFET is 0.5 V, when the device is biased at a gate voltage of 3 V, pinch-of would occur at a drain voltage of [ ]
    (a) 1.5 V (b) 2.5 V (c) 3.5 V (d) 4.5 V
19. The zero gate bias channel resistance of a junction field-effect transistor is 750 and the pinch-off voltage is 3V. For a gate bias of 1.5 V and very low drain voltage, the device would behave as a resistance of [ ]
    (a) 320 Ω (b) 816 Ω (c) 1000 Ω (d) l270 Ω

XII. WEBSITES:

1. http://www.onsemi.com
2. http://www.kpsec.freeuk.com/symbol.htm
3. http://buildinggadgets.com/index_circuitlinks.htm

4. http://www.guidecircuit.com

XIII. EXPERT DETAILS:

1. Dr. G. V. V. Sharma, Indian Institute of Technology, Hyderabad.
2. Dr. P. Sakthivel, Anna University, Chennai.
3. Dr. P. V. D. Somasekhar Rao (JNTUH)
4. Dr. T. Satya Savithri (JNTUH)
5. Dr. D. Rama Krishna (O.U)

XIV. JOURNALS:

1. IEEE Transaction on Electronic Devices
2. International Journal of Electronics (TF)
3. Active and Passive Electronic Components (Hindavi)
4. Journal of Active and Passive Electronic Devices
5. Journal of Electronic Testing
6. IETE Journal of Research
7. Journal of Electrical Engineering and Electronic Technology

XV. LIST OF TOPICS FOR STUDENT SEMINARS:

1. Formation of depletion layer in PN junction diode
2. Zener diode as voltage regulator
3. Common Collector Configuration
4. Need for biasing
5. Thermal runaway, thermal stability
6. Design of CE amplifier

XVII. CASE STUDIES / SMALL PROJECTS:

1. Voltage regulator
2. Regulated power supply
3. Single stage amplifier
4. SCR acts as fastest switch
5. FET act as a variable resistor