COMPUTER ORGANIZATION &OPERATING SYSTEMS (EC511PE)

COURSE PLANNER (2020-2021)

COURSE OBJECTIVE AND RELEVANCE:

1. To have a thorough understanding basic structure and operation of Digital Computer
2. Todiscussindetailtheoperationofthearithmeticunitincludingthealgorithms & implementation offixed-pointandfloating-pointaddition,subtraction, multiplication &division.
3. Tostudythehierarchicalmemorysystemincluding Cache MemoriesandVirtualMemory.
4. TostudythedifferentwaysofcommunicatingwithI/OdevicesandstandardI/Ointerfaces.
5. To implement the significant portion of an Operating Systems
6. To demonstrate the knowledge of function of Operating System, Memory Management, File Sharing and Interfaces

COURSE PURPOSE:

1. **Basic understanding of computer organization**: roles of processors, main memory, and input/output devices. Understanding the concept machine instruction. Understanding the relationship between assembly language and machine language; development of skill in assembly language programming; understanding the relationship between high-level compiled languages and assembly language. Understanding arithmetic and logical operations with integer operands. Understanding floating-point number systems and operation. Understanding simple data path and control designs for processors. Understanding memory organization, including cache structures and virtual memory schemes
2. **Operating Systems** is an essential part of any Computer-Science education. The purpose of this course is to understand the mechanisms of the Operating Systems like Process Management, Process Synchronization, Memory Management, File System Implementation, Storage Structures used in OS and Protection Principles. How effectively the OS is utilizing the CPU resources with the help of these mechanisms.

COURSE OUTCOME:

Students who have successfully completed this course will have full understanding of the
Following concepts

1. Learn the basic structure of a digital computer, Understand the arithmetic and logical operations of binary number system.
2. Understand the design of the Control unit.
3. Have knowledge about the organization of Arithmetic and Logical unit and I/O unit.

4. Understand the design of Memory unit, Learn the overview of computer system hardware
5. Learn about major activities of an OS with regard to file management, Learn the operating system functions

PRE-REQUISITES:

1. Computer Organization-Carl Hamacher.
2. Computer Systems Architecture-Moris Mano.
3. Computer Organization and Architecture -William Stallings, 6th Edition.
4. Structured Computer Organization-Andrew s. Tanenbaum.
5. Operating Systems-Stallings, 6th Edition-2009.
6. Operating System Concepts- Abraham Silberchatz, 8th Edition.

HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (PO)		Level	Proficiency assessed by
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineeringfundamentals, and an engineering specialization to the solution of complex engineering problems related to Electronics & Communication and Engineering.	3	Assignments, Exercises
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complexengineering problems related to Electronics & Communication Engineering and reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	3	Assignments
PO3	**Design/development of solutions**: Design solutions for complex engineering problems related to Electronics & Communication Engineering anddesign system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	2	Assignments, Exercises
PO4	**Conduct investigations of complex problems**: Use research-based knowledge and researchmethods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	3	Assignments

Program Outcomes (PO)		Level	Proficiency assessed by
PO5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modernengineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	2	Assignments, Seminars
PO6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assesssocietal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the Electronics & Communication Engineering professional engineering practice.	2	Seminars
PO7	**Environment and sustainability**: Understand the impact of the Electronics & Communication Engineering professional engineering solutionsin societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	1	Assignments, Seminars
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms ofthe engineering practice.	-	-
PO9	**Individual and team work**: Function effectively as an individual, and as a member or leader indiverse teams, and in multidisciplinary settings.	1	Oral Discussions
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineeringcommunity and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	2	Document Preparation, Presentation
PO11	**Project management and finance**: Demonstrate knowledge and understanding of theengineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	1	Assignments
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage inindependent and life-long learning in the broadest context of technological change.	2	Assignments

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes		Level	Proficiency assessed by
PSO 1	**Professional Skills:** An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of complex systems.	2	Lectures, Assignments
PSO 2	**Problem-Solving Skills:** An ability to solve complex Electronics and communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.	3	Tutorials
PSO 3	**Successful Career and Entrepreneurship:** An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.	2	Seminars, Projects

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

COURSE CONTENT:
JNTUH SYLLABUS

UNIT-1

Basic Structure Of Computers: Computer Types, Functional Unit, Basic Operation Concepts, Bus Structures, Software, Performance, Multiprocessors and Multi Computers, Data Representation, Fixed Point Representation, Floating Point Representation.

Register Transfer Language and Micro Operations: Register Transfer Language, Register Transfer Bus and Memory Transfer, Arithmetic Micro Operations, Logic Micro Operations, Shift Micro Operations, Arithmetic Logic Shift Unit, Instruction Codes, Computer Registers, Computer Instructions- Instruction Cycle.

Memory: Reference Instructions, Input – Output and Interrupt, STACK Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer.

UNIT-2

Micro Programmed Control: Control Memory, Address Sequencing, Micro program Examples, Design of Control Unit, Hard Wired Control and Micro programmed Control.
The Memory System: Basic Concepts OfSemi Conductor RAM Memories, Read Only Memories, Cache Memories and Performance Considerations, Virtual memories Secondary Storage, Introduction to Raid.

UNIT-3
Input–Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous Data Transfer Modes, Priority Interrupt, Direct Memory Access, Input-Output Processor (IOP), Introduction To Peripheral Components, Interconnect (PCI) Bus, Introduction To Standard Serial Communication Protocols Like RS232, USB and IEEE1394.

UNIT-4

Operating Systems Overview: Overview of Computer Operating Systems Functions, Protection and Security, Distributed System, Special Purpose Systems, Operating Systems Structure, Operating System Services and System Calls, System Programs, Operating System Generation.
Memory Management: Swapping, Contiguous Memory Allocation, Paging, Structure of Paging Table, Segmentation, Virtual Memory, Demand Paging, Page-Replacement Algorithms, Allocation Of Frames, Thrashing Case Studies – Unix, Linux, and Windows.

Principles of Deadlock: System Model, Deadlock Characterization, Deadlock Prevention, Detection and Avoidance, Recovery From Deadlock.

UNIT-5
File System Interface: The Concept of a File Access Methods, Directory Structure, File System Mounting, File Sharing , Protection.
File System Implementation: File System Structure, File System Implementation, Directory Implementation, Allocation Methods, Free- Space Management.

GATE SYLLABUS:
Computer Organization : Machine instructions and addressing modes, ALU and data path, CPU control design, Memory interface, I/O interface (Interrupt and DMA mode), Instruction pipelining, Cache and main memory, Secondary storage.

Operating System: Processes, Threads, Inter-process communication, Concurrency, Synchronization, Deadlock, CPU scheduling, Memory management and virtual memory, File systems, I/O systems, Protection and security.

IES SYLLABUS: Not Applicable

TEXT BOOKS:

1. Computer Organization- Carl Hamacher, ZvonksVranesic, Safeazaky, 5th Edition, Mcgraw Hill
2. Computer Systems Architecture- M. Morris Mano, 3rdEdition,Pearson
3. Operating System Concepts- Abraham Silberchatz,Peter B .Galvin,Greg Gagne, 8thEdition,John Wiley

REFERENCE BOOKS:

1. Computer Organization and Architecture- William Stallings 6th Edition, Pearson.
2. Structured Computer Organization- Andrew S. Taenbaum,4th Edition PHI.
3. Fundamentals of Computer Organization and Design-SivaraamaDandamudi Springer Interdiction.
4. Operating Systems- Internals And Design Principles, Stallings, 6th Edition-2009, Pearson Education.

LESSON PLAN:

Lecture No.	Unit No.	Topics to be covered	Link for PDF	Link for Small Projects/ Numericals(if any)	Course learning outcomes	Teaching Methodology	Reference
1	1	Unit1:**Basic structure of computers**: Computer types, Functional Unit, Basic	https://drive.google.com/file/d/1GzIkDCiS7gEhpBGK1RVasX49dQL-dlPO/view?usp=sharing	**https://www.electronicshub.org/arm-based-projects/**	Identify the basic elements of hardware and explain their functions and how they fit	PPT	**Morris-mano-Computer system Architecture**
2		Bus structures, Software, Software Performance	https://drive.google.com/file/d/1IQMh8ecEXIdV3yXNLWER0FOM0aaRIKtT/view?usp=sharing		Identify the basic elements of hardware and explain their functions and how they fit	PPT	
3		Fixed Point representation, Floating Point representation	https://drive.google.com/file/d/1MAvEXBIARR8k5LGw2xosv6M2ookaOQ9D/view?usp=sharing		Learn how data is represented, manipulated and stored within a	PPT	
4		Register Transfer Language and	https://drive.google.com/file/d/1j5uwQ6OLixQD	**http://krchowdhary.com/co/projects.**	Differentiate the Bus structures	PPT	

		Micro operations	dM3MXDNTtLWwBkUoBfCo/view?usp=sharing	**html**			
5		Bus and Memory Transfers	https://drive.google.com/file/d/19F7fGiFSeRopanNodSyfJw5ZyAArqvQc/view?usp=sharing		Differentiate the Bus structures	Chalk and Talk	
6		Arithmetic Micro operations, Logic Micro operations	https://drive.google.com/file/d/1M2DqbV8j9H8kqDBhddtWW5TVdjbRFMox/view?usp=sharing		Describe how arithmetic and logical operations are performed by computers	Chalk and Talk	
7		Shift Micro operations, Arithmetic Logic and Shift Unit	https://drive.google.com/file/d/1_Rb6U9vO_nxG6CSMHHygJPVcKONf0Jql/view?usp=sharing	**https://github.com/topics/computer-organization**	Shift unit design	Chalk and Talk	
8		Instruction codesS	https://drive.google.com/file/d/1Kz03eAclGJV5Y9SkxlQBPql8RI5_lKPZ/view?usp=sharing		Instruction codes	Chalk and Talk	
9		tack Organization ,Instruction Formats	https://drive.google.com/file/d/17my1LFT7VsfY4c6YsOuiDJZ8RUDzgcG3/view?usp=sharing		Understand Stack notations	PPT	
10		Addressing Modes ,Data Transfer and Manipulation	https://drive.google.com/file/d/1ZJy8haiCbvzenx-FP1eXA3yV5nQNgPEf/view?usp=sharing		understand differnt addressing modes	PPT	
11		Program Control, Reduced Instruction Set Computer.	https://drive.google.com/file/d/18cpVZZJLZoeWX5zWm48BxcJLkwWM8Pbb/vi	**https://github.com/topics/computer-organization**	Concept of RISC	PPT	

			ew?usp=sharing				
12		Unit2: **Micro Programmed Control**:	https://drive.google.com/file/d/18cpVZZJLZoeWX5zWm48BxcJLkwWM8Pbb/view?usp=sharing		Understand the Micro-code generation for the control memory	PPT	
13		Micro program Examples, Design Of Control Uni	https://drive.google.com/file/d/18cpVZZJLZoeWX5zWm48BxcJLkwWM8Pbb/view?usp=sharing		Undersatndmicro program examples	PPT	
15		**The Memory System:** Basic Concepts Of Semi-Conductor RAM Memories	https://drive.google.com/file/d/18cpVZZJLZoeWX5zWm48BxcJLkwWM8Pbb/view?usp=sharing		Understand the memory hierarchy and the function of RAM and ROM chips along with Connection between CPU and Memory	PPT	
16	**2**	Read Only Memories, Cache Memories Performance Considerations	https://drive.google.com/file/d/18cpVZZJLZoeWX5zWm48BxcJLkwWM8Pbb/view?usp=sharing		Describe Cache memory	Chalk and Talk	
17		Virtual Memories Secondary Storage	https://drive.google.com/file/d/18cpVZZJLZoeWX5zWm48BxcJLkwWM8Pbb/view?usp=sharing		Analyze the concept of virtual memory	Chalk and Talk	
18		UNIT 3 :**Input-Output Organization:Input-Output interface, Asynchronous data transfer Modes, Priority Interrupt**	https://drive.google.com/file/d/1CVAB_XJWglVKoUWseyyOEkAHfpiURTif/view?usp=sharing		Identify different ways of communicating with I/O devices	PPT	
19		Direct Memory	https://drive.goo	**http://krcho**	Describe Speed	PPT	

		Access,	gle.com/file/d/1CVAB_XJWglVKoUWseyyOEkAHfpiURTif/view?usp=sharing	**wdhary.com /co/projects. html**	of transfer using Direct Memory Access technique		
20		Input-Output Processor(IOP)	https://drive.google.com/file/d/1CVAB_XJWglVKoUWseyyOEkAHfpiURTif/view?usp=sharing		Communication between CPU and IOP	Chalk and Talk	
21		Serial communication, Introduction to peripheral components	https://drive.google.com/file/d/1UsOwj-V_NKHTiiKv0bkOzhL7C0S6H9HW/view?usp=sharing		Illustrate different Serial Communication Protocols	PPT	
22		Interconnect(PCI)bus, RS 232,USB,IEEE 1394	https://drive.google.com/file/d/1UsOwj-V_NKHTiiKv0bkOzhL7C0S6H9HW/view?usp=sharing		Illustrate different Serial Communication Protocols	PPT	
23		UNIT 4 :**Operating Systems Overview:** Overview of Computer Operating Systems Functions	https://drive.google.com/file/d/1ssHvHdaZuhhTyAD1Qg0dV4zkxGnB8Ri9/view?usp=sharing		Understand the purpose of the operating system.	PPT	Operating System Concepts- Abraham Silberchatz, Peter, John Wiley
24		Protection And Security	https://drive.google.com/file/d/1ssHvHdaZuhhTyAD1Qg0dV4zkxGnB8Ri9/view?usp=sharing		To know protection and security issues	PPT	
25		Distributed System,	https://drive.google.com/file/d/1ssHvHdaZuhhTyAD1Qg0dV4zkxGnB8Ri9/view?	**https://www .electronicshub.org/arm-based-projects/**	To distiguish distributed system	Chalk and Talk	

			usp=sharing				
26	**3**	Special Purpose Systems	https://drive.google.com/file/d/1ssHvHdaZuhhTyAD1Qg0dV4zkxGnB8Ri9/view?usp=sharing		To understand special purpose systems	PPT	
27		Operating Systems Structure	https://drive.google.com/file/d/1ssHvHdaZuhhTyAD1Qg0dV4zkxGnB8Ri9/view?usp=sharing		To understand the OS	PPT	
28		Operating System Services and System Calls	https://drive.google.com/file/d/1ssHvHdaZuhhTyAD1Qg0dV4zkxGnB8Ri9/view?usp=sharing		To understand OS services	PPT	
29		System Programs	https://drive.google.com/file/d/1ssHvHdaZuhhTyAD1Qg0dV4zkxGnB8Ri9/view?usp=sharing		To understand system programs	PPT	
30		Operating System Generations	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing		To understand development of os	Chalk and Talk	
31		Memory Management: Swapping	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing		To understand the ARM Register	Chalk and Talk	Operating System Concepts- Abraham Silberchatz, Peter, John Wiley
32		Contiguous Memory Allocation	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharin		fragmentation	PPT	

			g				
33		Paging, Structure Of Paging Table ,Segmentation	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing		demand paging and diferent page replacement algorithms	PPT	
34	**4**	Virtual Memory	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing		To understand virualmemory,adress space	PPT	
35		Demand Paging	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing		demand paging and diferent page replacement algorithms	PPT	
36		Page-Replacement Algorithms,	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing	https://awesomeopensource.com/projects/computer	demand paging and diferent page replacement algorithms	PPT	
37		Allocation Of 4-8-16Frames Thrashing Case Studies – Unix, Linux, and Windows.	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing		Case studies:building of unix and windows os		
38		Principles Of Deadlock: System Model ,Deadlock Characterization	https://drive.google.com/file/d/1YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing		To Understand the Thumb instructions	PPT	
39		Deadlock Prevention	https://drive.google.com/file/d/1	**https://www.electronicsh**	To deadlock prevention	PPT	

			YX1fcn-NrJxjJiSCXC7q8ySbMK9slrQH/view?usp=sharing	**ub.org/arm-based-projects/**	mechanisms		
40	**5**	UNIT 5 : **File system Interface:** The concept of a file	https://drive.google.com/file/d/10w3nn-paglVeYNK5DUcIM23vwdy8PHfI/view?usp=sharing		Different types of files FAT/NTFS	Chalk and Talk	
41		File system Mounting	https://drive.google.com/file/d/10w3nn-paglVeYNK5DUcIM23vwdy8PHfI/view?usp=sharing	**https://www.electronicshub.org/arm-based-projects/**	File mounting	PPT	
42		File sharing, Protection	https://drive.google.com/file/d/10w3nn-paglVeYNK5DUcIM23vwdy8PHfI/view?usp=sharing		protection mechanisms	PPT	
43		File System Implementation Directory Implementation	https://drive.google.com/file/d/1fAfiwAtSYeEZe4J3ArdirNRz4kWE9o7S/view?usp=sharing		To Understand file system implementation	PPT	

TEXT BOOKS:

1. Computer Organization –Carl Hamacher,Zvons,5th Edition, McGraw Hill

2.mputer Systems Architecture-M. Morris Mano, 3rd Edition, Person

3.rating System Concepts-Abraham Silberchatz, Peter, John Wiley

MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

Course	Program Outcomes	Program Specific Outcomes

Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	S	H	H	S	S								H	S	
CO2		H	S										S	H	
CO3		H	S										S	H	
CO4	S	S	S	S								S	H	S	
CO5	S	S	S	S	S								H	S	S

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) - : None

QUESTION BANK:

DESCRIPTIVE QUESTIONS

UNIT 1:

Short answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1	Explain the role of program counter in Instruction execution?	Understand	1
2	Explain the role of program counter in Instruction execution?	Understand	1
3	Describe the basic functional units of a computer?	Understand	1
4	Define memory access time.	Remember	1
5	Explain memory address register (MAR) and memory data register (MDR)?	Understand	2
6	Define two techniques used to increase the clock rate R?	Remember	1

Long answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome

1	Explain the functional organization of a digital computer and explain the function of each element of a computer.	Understand	2
2	Illustrate the diagram for connection between the processor and the memory and explain basic operational concepts of computer.	Understand	1
3	Explain about various buses such as internal, external, back plane, I/O System, address, data, synchronous	Understand	1
4	Define system software? Explain various functions of systems software.	Remember	1
5	The following transfer statements specify a memory. Explain the memory operation in each case. a) R<-M[AR] b) M[AR]<-R3 c) R<-M[R5]	Understand	2
6	Discuss briefly about Floating point Representation with Example	Understand	1
7	Explain the following related to Stack Organization. a)Register Stack b)Memory Stack	Understand	2
8	Show how can the following operation be performed using: a-three address instruction b- two address instruction c- one address instruction d- zero address instruction X = (A + B) * (C + D)	Knowledge	1
9	Explain briefly about RISC architecture.	Understand	2
10	List and explain conditional branch instructions?	Knowledge	1

UNIT-2:

Short answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1.	Describe the two approaches used for generating the control signals in proper sequence.	Understand	2
2.	Define the following: (a) Micro-operation (b) Micro-instruction (c) Micro- program (d) Micro-code.	Remember	1

3.	Explain the factors to determine the control signals?	Understand	2
4.	Discuss the features of the hardwired control?	Understand	2
5.	Define micro programmed control?	Remember	1

Long Answer Questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1.	Define Control memory? Explain Micro programmed Control Organization.	Remember	1
2.	Explain the following related to Address Sequencing. a)Conditional branching b)Mapping of Instruction	Understand	2
3.	Explain the Organization of Hardwired control in detail.	Understand	2
4.	Explain briefly about Micro-program Sequencer with diagram.	Understand	2
5.	Explain the memory hierarchy with the reference of following metrics? A)Speed b) Cost c) Size	Understand	2
6.	Explain organization of a 1 K X 1 memory chip with neat diagram.	Understand	2
7.	Explain i) ROM ii) PROM iii) EPROM iv) EEPROM.	Understand	2
8.	Explain the following Cache Mapping Techniques (a) Direct Mapping (b) Set Associative Mapping.	Understand	2
9.	Explain briefly about a) Hit Rate b) Miss Penalty with Examples.	Understand	2
10.	Define Page-fault? Explain the following page replacement algorithms with Examples a)FIFO b)LRU	Remember	1

UNIT-3:

Short answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1	Write about Memory Hierarchy?	Remember	3

2	Explain RAM and ROM?	Understand	3
3	Write about Auxiliary Memory?	Remember	3
4	Explain about Cache Memory?	Understand	3
5	Write about Associate Memory?	Remember	3

Long answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1	Distinguish between memory mapped I/O and I/O mapped I/O.	Understand	3
2	Differentiate isolated I/O and memory mapped I/O?	Analyze	3
3	Explain briefly about Asynchronous communication interface with diagram.	Understand	2
4	Discuss DMA transfer technique in detail with block diagram?	Understand	3
5	Explain the following A) CPU-IOP communication B) Daisy- Chaining priority c) Bit-oriented protocol	Understand	3
6	Define Page-fault? Explain the following page replacement algorithms with Examples a)FIFO b)LRU	Remember	3
7	Discuss the following a) Interrupt-initiated I/O b) Interrupt Cycle	Understand	3
8	Discuss USB Serial communication protocol in detail	Understand	3
9	Draw and Explain the Connection of I/O bus to input-output devices	Remember	3
10	Explain briefly about Input-output Processor with Diagram	Understand	3

UNIT-4:

Short Answer Questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1	Define Operating System? Explain the three main purposes of	Remember	4

	an operating system?		
2	Define kernel? List at least two functions of the kernel.	Remember	4
3	Define thread? Explain about multithreading.	Remember	4
4	Describe the process state diagram	Remember	4
5	Explain the advantages of Multiprogramming	Understand	4

Long answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1	What are the various components of operating system structure? Explain the simple and Layered approach of operating system in details.	Understand	3
2	What is a system call? Explain how a user application invoking the open () system call is handled.	Understand	4
3	What is paging? Explain the basic method for implementing paging.	Understand	4
4	Explain any 4 page replacement algorithms with diagrams.	Understand	3
5	Explain the following: a) Fragmentation b) First fit c) Best fit d) Worst fit e)Segmentation	Understand	3
6	Describe the operating system structures	Remember	4
7	Differentiate between internal and external fragmentation. Which one occurs in paging scheme?	Analyze	4
8	Define page fault? When does a page fault occur? Describe the action taken by OS when page fault occurs.	Remember	4
9	Explain the basic Scheme of page replacement and about the various page replacement strategies with examples.	Understand	4
10	Define deadlock? What are the four conditions necessary for deadlock? How it can be prevented.	Remember	4

UNIT-5:

Short answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1	Define a file?	Remember	5
2	List the various file attributes.	Remember	5

3	Discuss the various file operations?	Understand	5
4	Describe the layout of a file system?	Remember	5
5	State the information associated with an open file?	Remember	5

Long answer questions

S.NO	Question	Blooms Taxonomy Level	Course Outcome
1	Explain sequential and indexed file access methods.	Understand	2
2	Explain the three allocation methods in file system implementation Illustrate with proper	Understand	2
3	Write short notes on A. File sharing B. Protection	Remember	5
4	Explain the indexed allocation method with neat diagram.	Understand	2
5	Draw the diagrams for the following and explain: A. A typical file-system organization B. Single-level directory C. Two-level directory	Remember	5
6	Explain briefly about Acyclic-Graph Directories structure with diagram.	Understand	2
7	Explain in detail about File sharing and protection?	Understand	2
8	Define Free-Space list? Explain different implementation methods for free space management?	Remember	1
9	Discuss the following a)File attributes b)File types c)Internal File structure	Knowledge	4
10	Explain briefly about virtual File system with diagram?	Understand	2

OBJECTIVE TYPE QUESTIONS:

UNIT I

1. The decoded instruction is stored in _____ .
   a) IR
   b) PC
   c) Registers
   d) MDR
2. Which registers can interact with the secondary storage ?
   a) MAR
   b) PC

c) IR
d) R0

3. The instruction -> Add LOCA,R0 does,
   a) Adds the value of LOCA to R0 and stores in the temp register
   b) Adds the value of R0 to the address of LOCA
   c) Adds the values of both LOCA and R0 and stores it in R0
   d) Adds the value of LOCA with a value in accumulator and stores it in R0
4. The internal Components of the processor are connected by _____ .
   a) Processor intra-connectivity circuitry
   b) Processor bus
   c) Memory bus
   d) Ram bus
5. When generating physical addresses from logical address the offset is stored in _____.
   a) Translation look-aside buffer
   b) Relocation register
   c) Page table
   d) Shift register
6. During the execution of a program _____ gets initialized first (program counter)
7. _____ is used to choose between incrementing the PC or performing ALU (multiplexer)
8. _____ is used to store data in registers (D flip flop)
9. The unit which acts as an intermediate agent between memory and backing store to reduce process time is _____ .(cache)
10. The BOOT sector files of the system are stored in _____ .(rom)

UNIT II

1. In micro-programmed approach, the signals are generated by _____.
   a) Machine instructions
   b) System programs
   c) Utility tools
   d) None of the above
2. A word whose individual bits represent a control signal is _____.
   a) Command word
   b) Control word
   c) Co-ordination word
   d) Generation word
3. A sequence of control words corresponding to a control sequence is called _____.
   a) Micro routine
   b) Micro function

c) Micro procedure
d) None of the above

4. Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is _____.
   a) Horizontal organization
   b) Vertical organization
   c) Diagonal organization
   d) None of the above
5. The case/s where micro-programmed cannot perform well
   a) When it requires to check the condition codes
   b) When it has to choose between the two alternatives
   c) When it is triggered by an interrupt
   d) Both a and b
6. Individual control words of the micro routine are called as _____.(micro instruction)
7. The special memory used to store the micro routines of a computer is _____.(control store)
8. Every time a new instruction is loaded into IR the output of _____ is loaded into UPC.(starting address generator)
9. Complete the following analogy :- Registers are to RAM's as Cache's are to _____ .(TLB)
10. _____ is used to effectively utilize main memory(dynamic loading)

UNIT III

1. The DMA differs from the interrupt mode by
   a) The involvement of the processor for the operation
   b) The method accessing the I/O devices
   c) The amount of data transfer possible
   d) Both a and c
2. The DMA transfers are performed by a control circuit called as
   a) Device interface
   b) DMA controller
   c) Data controller
   d) Over looker
3. The DMA controller has _____ registers
   a) 4
   b) 2
   c) 3
   d) 1

4. The system developed by IBM with ISA architecture is _____.
   a) SPARC
   b) SUN-SPARC
   c) PC-AT
   d) None of the above
5. The primary function of the BUS is
   a) To connect the various devices to the CPU
   b) To provide a path for communication between the processor and other devices
   c) To facilitate data transfer between various devices
   d) All of the above
6. The controller is connected to the ____(system bus)
7. The controller uses _____ to help with the transfers when handling network interfaces.(input buffer storage)
8. To overcome the conflict over the possession of the BUS we use _____(BUS arbitrators)
9. _____ is used as an intermediate to extend the processor BUS.(bridge)
10. _____ is an extension of the processor BUS.(PCI BUS)

UNIT IV

1. CPU fetches the instruction from memory according to the value of
   a) program counter
   b) status register
   c) instruction register
   d) program status word
2. A memory buffer used to accommodate a speed differential is called
   a) stack pointer
   b) cache
   c) accumulator
   d) disk buffer
3. Which one of the following is the address generated by CPU?
   a) physical address
   b) absolute address
   c) logical address
   d) none of the mentioned
4. The wait-for graph is a deadlock detection algorithm that is applicable when :
   a) all resources have a single instance
   b) all resources have multiple instances
   c) both a and b
   d) None of the above

5. The disadvantage of invoking the detection algorithm for every request is :
   a) overhead of the detection algorithm due to consumption of memory
   b) excessive time consumed in the request to be allocated memory
   c) considerable overhead in computation time
   d) All of these
6. Cache memory is used in a computer system to ----------(Speed up memory Access)
7. Program which acts as a interface between a user and the hardware is called ----------- (Operating system)
8. ----------is a program that translates mnemonic statements into executable instructions.(Assembler)
9. If the set of resources available to the process is fixed throughout the process's lifetime then its domain is(static)
10. In I/O protection I/O must be performed via_____(system calls)

UNIT V

1. Data cannot be written to secondary storage unless written within a _____.
   a) file
   b) swap space
   c) directory
   d) text format
2. The information about all files is kept in :
   a) swap space
   b) operating system
   c) separate directory structure
   d) None of these
3. The open file table has a/an _____ associated with each file.
   a) file content
   b) file permission
   c) open count
   d) close count
4. 4) Sequential access method _____ , on random access devices.
   a) works well
   b) doesn't work well
   c) Both a and b
   d) None of these
5. For a direct access file :
   a) there are restrictions on the order of reading and writing
   b) there are no restrictions on the order of reading and writing

c) access is restricted permission wise
d) access is not restricted permission wise

6. The larger the block size, the _____ the internal fragmentation.(greater)
7. The direct access method is based on a _____ model of a file, as _____ allow random access to any file block.(disk , disks)
8. An unrecoverable error is known as _____.(hard error)
9. Using swap space significantly _____ system performance.(decreases)
10. It is _____ to reread a page from the file system than to write it to swap space and then to reread it from there.(more efficient)

GATE QUESTIONS:

1. The most widely used code that represents each character as a unique 8-bit code is:
   (A) ASCII.
   (B) Unicode.
   (C) Binary numbering system.
   (D) EBCDIC
2. Zero address instruction format is used for
   (A) RISC architecture.
   (B) CISC architecture.
   (C) Von-Neuman architecture.
   (D) Stack-organized architecture.
3. Stack overflow causes
   (A) Hardware interrupts.
   (B) External interrupts.
   (C) Internal interrupts.
   (D) Software interrupts.
4. Address symbol table is generated by the
   (A) Memory management software. (B) Assembler.
   (C) Match logic of associative memory. (D) Generated by operating system
5. If a user needs information instantly available to the CPU, it should be stored:
   (A) in the CPU.
   (B) in RAM.
   (C) in secondary storage.
   (D) on a CD.
6. A CPU generates 32 bit virtual addresses, the page size is 4KB, the processor has a TLB which can hold a total of 128 page table entries and is 4 way set associative. What will be the minimum size of TLB tag
   (A) >11 bits
   (B) >13 bits
   (C) >15 bits
   (D) >20 bits
7. In a non-vectored interrupt, the address of interrupt service routine is

(A) Obtained from interrupt address table.
(B) Supplied by the interrupting I/O device.
(C) Obtained through Vector address generator device.
(D) None of the above

8. A scheduling algorithm assigns priority proportional to the waiting time of a process. Every process starts with priority zero(the lowest priority). The scheduler re-evaluates the process priorities every T time units and decides the next process to schedule. Which one of the following is TRUE if the processes have no I/O operations and all arrive at time zero?
   (A) This algorithm is equivalent to the first-come-first-serve algorithm
   (B) This algorithm is equivalent to the round-robin algorithm
   (C) This algorithm is equivalent to the shortest-job-first algorithm
   (D) This algorithm is equivalent to the shortest-remaining-time-first algorithm
9. A thread is usually defined as a 'light weight process' because an operating system (OS) maintains smaller data structures for a thread than for a process. In relation to this, which of the followings is TRUE?
   (A) On per-thread basis, the OS maintains only CPU register state
   (B) The OS does not maintain a separate stack for each thread
   (C) On per-thread basis, the OS does not maintain virtual memory state
   (D) On per thread basis, the OS maintains only scheduling and accounting information
10. Let the page fault service time be 10ms in a computer with average memory access time being 20ns. If one page fault is generated for every 106 memory accesses, what is the effective access time for the memory?
    (A) 21ns (B) 30ns (C) 23ns (D) 35ns
11. Consider the following table of arrival time and burst time for three processes P0,P1 and P2.Process Arrival time Burst Time P0 0 ms 9 ms P1 1 ms 4ms P2 2 ms 9ms The pre-emptive shortest job first scheduling algorithm is used. Scheduling is carried out only at arrival or completion of processes. What is the average waiting time for the three processes?
    (A) 5.0 ms (B) 4.33 ms (C) 6.33 ms (D) 7.33 ms
12. Consider the following statements about user level threads and kernel level threads. Which one of the following statements is FALSE?
    (A) Context switch time is longer for kernel level threads than for user level threads.
    (B) User level threads do not need any hardware support.
    (C) Related kernel level threads can be scheduled on different processors in a multi-processor system.
    (D) Blocking one kernel level thread blocks all related threads.
13. An operating system uses Shortest Remaining Time first (SRT) process scheduling algorithm. Consider the arrival times and execution times for the following processes: Process Execution time Arrival time P1 20 0 P2 25 15 P3 10 30 P4 15 45.What is the total waiting time for process P2?
    (A) 5 (B) 15 (C) 40 (D) 55
14. A virtual memory system uses First In First Out (FIFO) page replacement policy and allocates a fixed number of frames to a process. Consider the following statements:

P: Increasing the number of page frames allocated to a process sometimes increases the page fault rate.
Q: Some programs do not exhibit locality of reference.
Which one of the following is TRUE?

(A) Both P and Q are true, and Q is the reason for P
(B) Both P and Q are true, but Q is not the reason for P.
(C) P is false, but Q is true
(D) Both P and Q are false.

15. A multi-user, multi-processing operating system cannot be implemented on hardware that does not support
    (A) Address translation
    (B) DMA for disk transfer
    (C) At least two modes of CPU execution (privileged and non-privileged)
    (D) Demand paging
16. Which of the following is/are advantage of virtual memory?
    (A) Faster access to memory on an average.
    (B) Processes can be given protected address spaces.
    (C) Linker can assign addresses independent of where the program will be loaded in physical memory.
    (D) Programs larger than the physical memory size can be run.
17. Which of the following actions is/are typically not performed by the operating system when switching context from process A to process B?
    (A) Saving current register values and restoring saved register values for process
    (B) Changing address translation tables.
    (C) Swapping out the memory image of process A to the disk.
    (D) Invalidating the translation look-aside buffer.

WEBSITES:

1. www.ioenotes.edu.np
2. www.tutorialspoint.com
3. www.srmuniv.ac.in
4. www.stat.auckland.ac.nz
5. williamstallings

EXPERT DETAILS:

1. Prof. M. Gopal, Department of Electrical Engineering, IIT Delhi
2. Prof. S.D. Agashe, Department of Electrical Engineering, IIT Bombay
3. Prof. S. Majhi, Department of Electrical Engineering, IIT Guwahati
4. Dr. IndraniKar, Department of Electrical Engineering, IIT Guwahati

JOURNALS:

1. IEEE compuert organization Magazine
2. International Journal of Systems, compuert organization
3. The International Journal of compuert organization

4. ICGST International Journal on computer Engineering
5. Journal of computer organization

LIST OF TOPICS FOR STUDENT SEMINARS:

1. Floating point Arithmetic operations, Decimal Arithmetic unit Decimal Arithmetic
2. operations
3. Virtual memories, secondary storage Introduction to RAID(Redundant Array of
4. Inexpensive Disks)
5. Protocols like RS232, USB, and IEEE1394.
6. CPU Scheduling.
7. Synchronization
8. Memory Scheduling.
9. Disk Scheduling.
10. File Systems Inter Process Communication.

CASE STUDIES / SMALL PROJECTS:

1. Virtual Machines
2. Run-Time Storage Management
3. Memory System Organization and Architecture
4. Tasking and Processes
5. Device Management
6. Digital Logic
7. Prepare A Case Study on Security Features Comparison of UNIX, LINUX, DOS and Windows Operating System.
8. Prepare a Project Report on How Scheduling Algorithms are Used in a Manufacturing Industry.